CONTROL DATA CORPORATION

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PRODUCT SPECIFICATION
FOR
FLEXIBLE DISK DRIVE
MODEL 9409T
(96 TPI)

MAGNETIC PERIPHERALS INC.
A subsidiary of CONTROL DATA CORPORATION

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1.0 GENERAL DESCRIPTION

The 9409T is a 96 TPI double-sided 5.25-inch flexible disk drive (FDD) which features one megabyte capacity. The 9409T utilizes standard 96 TPI double-sided 5.25-inch flexible media in either single density (FM) or double density (MFM) recording. Device applications include small computer systems, intelligent data terminals, and home computers. The 9409T is illustrated in Figure 1.

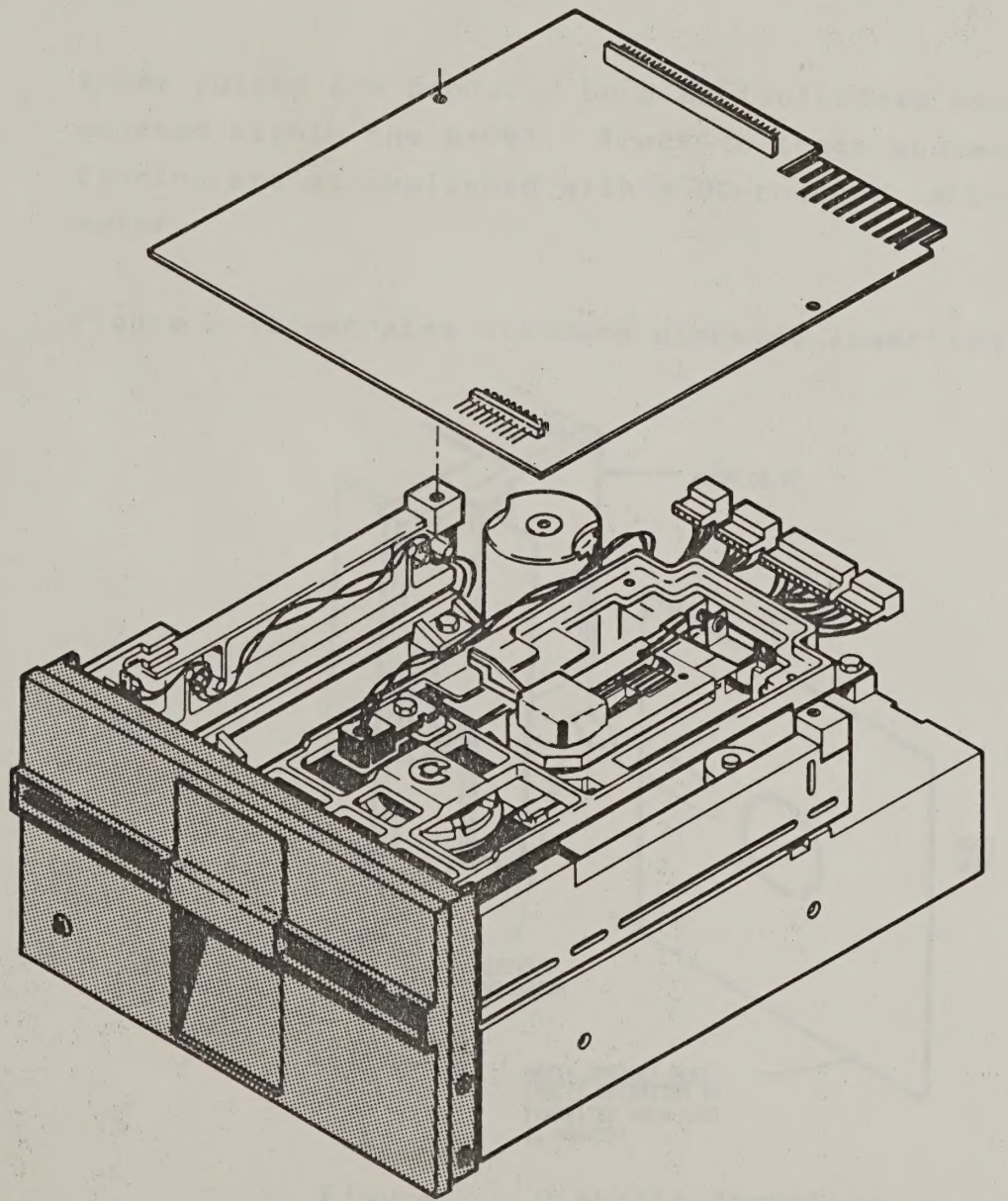

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Figure 1. 9409T Flexible Disk Drive

The 9409T contains control and read/write electronics and a band stepper track accessing positioner capable of reading o writing 96 tracks per inch. The 9409T incorporates tunnel erase heads which provide maximum signal to noise ratio.

The interface signals and timings, power requirements, mecha cal dimensions, and mounting requirements are industry-compa ble.

Index pulses are produced by a photoelectric sensing assemb mounted within the 9409T. Track-to-track accessing and pos: tioning are accomplished with a DC-powered, +12-volt steppe motor.

Figure 2 illustrates standard diskette insertion.

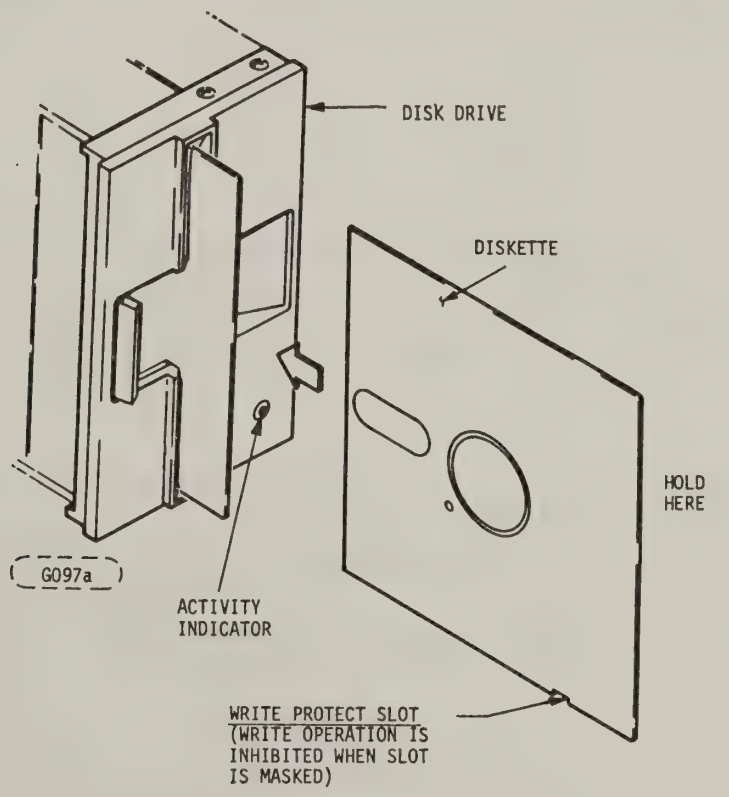


Figure 2. Diskette Insertion

2.0 APPLICABLE DOCUMENTS

2.1 STANDARDS

The Model 9409T FDD has been designed as a system peripheral to the highest standards of design and construction. The drive, however, must depend upon its host equipment to receive adequate power and environment in order to provide optimum performance and compliance with applicable industry and governmental regulations. Special attention must be given in the areas of safety, power distribution, grounding, shielding, audible noise control, and temperature regulation of the device to ensure specified performance and compliance with all applicable regulations.

The 9409T is a component, and, as such, is not subject to standards imposed by FCC Docket 20780/FCC 80-148 Part 15 governing EMI of computing devices.

2.2 DOCUMENTATION

The following documents and specifications provide detailed theory of operation, maintenance procedures, and media format considerations. These documents are not included with each unit, but must be ordered separately.

- Model 9409T FDD Hardware Maintenance Manual, 77653480
- Application Note, PLO and Write Precompensation for 5.25-Inch Flexible Disk Drives, 77653447
- Application Note, 5.25-Inch FDD Format Considerations and Controller Compatibilities, 75897469

3.0 FEATURES

3.1 STANDARD FEATURES

The 9409T FDD has the following standard features:

- Double-Sided 96 TPI 5.25-Inch Media Capability
- Single-Density (FM) and Double-Density (MFM) Encoding
- Industry-Compatible Interface
- Industry-Compatible Mounting Configurations
- Only Two DC Power Voltages Required (+5 V and +12 V)
- Write Protect Indication
- Activity Indicator
- Long-Life Ceramic Read/Write Heads
- Band Stepper Motor
- Hard or Soft Sector Formatting
- Head Select
- Drive Select
- Track-Zero Detection/Track-Zero Stop
- Index Detection
- Step/Direction Control for Track-to-Track Access
- Black Finish

3.2 OPTIONAL FEATURES

- Door Closed/Ready
- Head Load Solenoid

4.0 PERFORMANCE SPECIFICATIONS

Capacity	Single Density	Double Density
Unformatted		
Per Disk	500.0 kbytes	1.0 Mbyte
Per Surface	250.0 kbytes	500.0 kbytes
Per Track	3.125 kbytes	6.250 kbytes
Formatted (16 Sectors, 128/256 Bytes)*		
Per Disk	327.68 kbytes	655.36 kbytes
Per Surface	163.84 kbytes	327.68 kbytes
Per Track	2048 bytes	4096 bytes
Code	FM	MFM
Transfer Rate	125 kbits/s	250 kbits/s
Latency (Average)	100 ms	100 ms
Seek Time		
Track-to-Track	5 ms	5 ms
Average	132 ms	132 ms
Settle Time	15 ms	15 ms
Head-Load Time	0 (or 50 ms optional**)	0 (or 50 ms optional**)
Side-Select Time	200 µs***	200 µs***
Write Precompensation	0	250 ns (trk 43-79)

* Assumes tunnel erase heads.

** 50 ms with Head-Load Solenoid option.

*** Assumes motor on, drive selected, head loaded, and erase turn-off delay completed from any previous write operation.

4.1 DEFINITIONS

4.1.1 Latency

Latency is the time required for the read/write head to reach a particular area on a track after positioning is completed. For a rotational/spindle speed of 300 revolutions per minute, the 9409T has an average latency of 100 ms.

4.1.2 Seek/Settle Time

The seek/settle time is the time required by the read/write head to move from track to track plus the time needed for the head to stabilize on track prior to data transfer. Seek/settle time for the 9409T is 20 milliseconds: 5 milliseconds for a single track access and 15 milliseconds for head settling time.

4.1.3 Head-Load Time

Head-load time is defined as the time from initial activation of the head-load function until valid data transfer between the drive and controller can be assured. The 9409T requires no head load time. However, a head load solenoid is optional and can be supplied to customers on request. With the optional head-load solenoid, the amount of head-load time required by the 9409T is 50 milliseconds.

4.1.4 Read Stabilization

Upon conclusion of a write operation, a minimum delay time of 1 millisecond is required before valid read data can be assured. Time is required to allow for completing the erase function. Time necessary to allow for the read circuit to stabilize after switching from one head to the other is 200 microseconds.

The following MTBF assumes spindle drive motor duty cycle is 25% of power-on hours.

Error Rates	
Soft Read Errors	≤ 1 per 10^9 bits read
Hard Read Errors	≤ 1 per 10^{12} bits read
Seek Errors	≤ 1 per 10^6 seeks
MTBF	$\geq$8000 Power-On Hours, 25% Duty Cycle
MTTR	0.5 Hour
Service Life	5 Years
Preventive Maintenance	None Required

6.1 MEAN TIME BETWEEN FAILURES (MTBF)

The following equation defines MTBF:

$$\text{MTBF} = \frac{\text{Power On Hours}}{\text{Number of Equipment Failures}}$$

Power On Hours are defined as the total time which the drive has DC power applied, less maintenance time.

Equipment Failures are defined as any substandard performance of the drive because of equipment malfunction, excluding stoppages or substandard performance caused by operator error, adverse environment, power failure, controller failure, cable failure, or other failure not caused by the drive. In order to calculate a meaningful MTBF, all sites in which the drive is utilized is included and total power on hours should exceed 10,000 hours.

6.2 MEAN TIME TO REPAIR (MTTR)

Mean Time to Repair (MTTR) is defined as the average time required for an adequately trained and competent service technician to diagnose and correct a malfunction on site. MTTR for the 9409T is 30 minutes and does not include travel time nor time when the drive is not released to the service technician.

6.3 SERVICE LIFE

The 9409T has a useful service life of five years or 31,200 hours, whichever occurs first, before requiring factory overhaul. Repair or replacement of field replaceable parts is permitted during the lifetime of the drive.

7.0 PHYSICAL/ELECTRICAL SPECIFICATIONS

7.1 DC POWER REQUIREMENTS

DC power requirements are as shown in Table 1.

Table 1. DC Power Requirements

CONDITIONS	NOMINAL VOLTAGE		
	+5 V	+12 V	
		WITH HEAD LOAD SOLENOID	WITHOUT HEAD LOAD SOLENOID
Tolerance	±0.25 V	±0.6 V	±0.6 V
Ripple (Peak-to-Peak)	≤50 mV	≤100 mV	≤100 mV
Seeking Current:			
Typical:	0.5 A	0.9 A	0.75 A
Maximum Surge on Motor Start **	*0.7 A	*1.8 A	*1.65 A

* Specified current requirements are on a per-drive basis. Current requirement increases by a factor equal to the number of drives per power supply. For example, two drives per supply would require +12 V at 3.6 A and +5 V at 1.4 A.

**Typical surge duration is less than 200 milliseconds.

7.2 POWER DISSIPATION

With Head Load Solenoid	Without Head Load Solenoid
26.4 watts (maximum)*	24.5 watts (maximum)*
13.3 watts (nominal)	11.6 watts (nominal)

7.3 INRUSH CURRENT

Inrush current is dependent upon the power source as well as the 9409T. Primary considerations are host power supply source impedance(s), host-to-9409T power line resistance and inductance, and 9409T capacitance load presented by the filter capacitors. Schematically, this may be represented as shown in Figure 3.

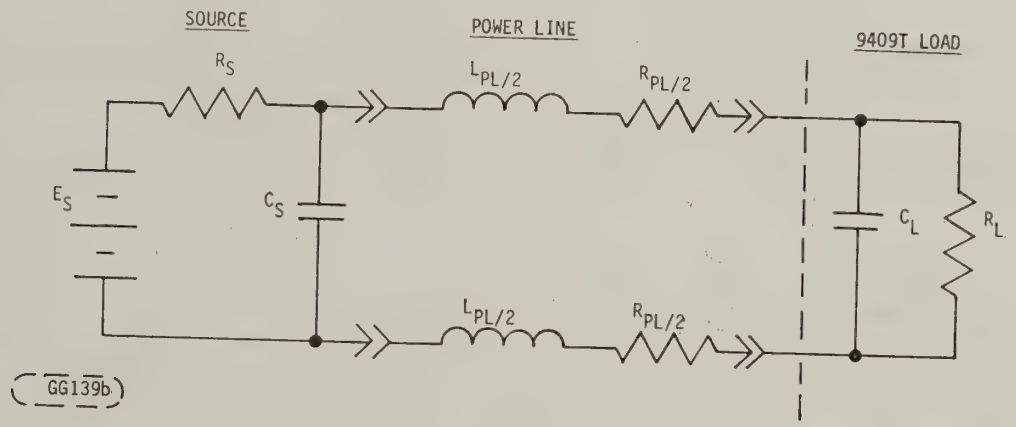


Figure 3. Inrush Current

Nominal equivalent loads for the 9409T are as follows:

	+12 V	+5 V
C_L	22 microfarads	39 microfarads
R_L	13 ohms	10 ohms

* Maximum power dissipation is calculated using maximum current surge and upper tolerance on power supply voltage rating. The peak value is typically 100 ms after motor start and has a duration less than 200 ms.

7.4 ENVIRONMENTAL LIMITS

Temperature and humidity specifications preclude condensation on any drive part. The 9409T is intended for use with host systems which operate in computer room and office environments. Altitude and barometric pressure specifications are referenced to a standard day at 58.7°F (14.8°C).

	Operating	Shipping and Storage
Ambient Temperature	40° to 115°F (4.4° to 46.1°C)	-40° to 144°F (-40° to 62.2°C)
Temperature Gradient	18°F/hr (10°C/hr)	36°F/hr (20°C/hr)
Relative Humidity	20% to 80%	0 to 95%
Maximum Wet Bulb Temperature	79°F (26.1°C)	No condensation
Altitude (Sea Level Reference)	-983 to +9850 feet (-300 to +3002 meters)	-983 to +9850 feet (-300 to +3002 meters)
Barometric Pressure		
in of Hg	22.2 to 30.9	18.8 to 30.9
mm of Hg	563.6 to 784.9	477.5 to 784.9
psi	10.9 to 15.18	9.22 to 15.18

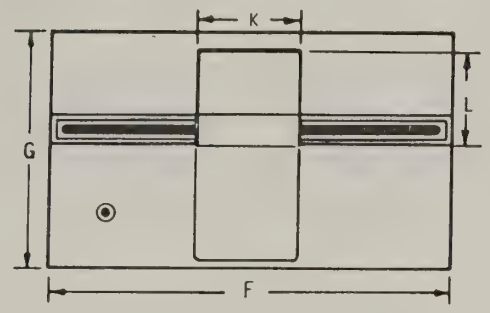
7.5 MECHANICAL SPECIFICATIONS

Following are mechanical specifications for the 9409T. Refer to Figure 4 for detailed mounting dimensions.

Height:	3.38 inches	85.8 millimeters
Width:	5.88 inches	149.4 millimeters
Depth:	8.29 inches	210.6 millimeters
Weight:	3.2 pounds	1.45 kilograms

WT: 3.2 lbs. (1.45 kg)

MOUNTING HOLES: FOUR ON BOTTOM, TWO EACH SIDE; #6-32 X 0.31 in. (7.9 mm) DEPTH



PACKAGE DIMENSION		
	INCHES	MILLIMETERS
A	8.00 MAX	203.2 MAX
B	5.75 +0.00 -0.02	146 +0.00 -0.5
C	0.19 ±0.02	4.5 ±0.5
D	1.87 ±0.02	47.5 ±0.5
E	3.12 ±0.02	79.2 ±0.5
F	5.88 ±0.01	149.4 ±0.3
G	3.38 ±0.01	85.9 ±0.3
H	0.06 ±0.01	1.5 ±0.3
I	5.50 ±0.02	140 ±0.5
J	0.86 ±0.02	21.8 ±0.5
K	1.50 ±0.01	38.1 ±0.5
L	1.41 ±0.01	35.8 ±0.5
M	0.29 ·0.02	7.4 ·0.5

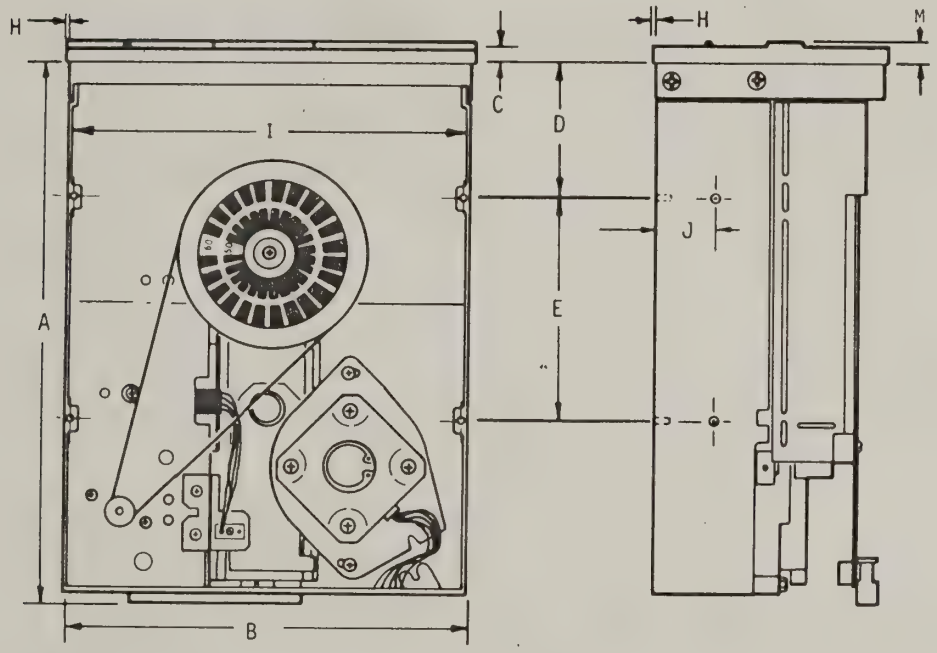


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Figure 4. Dimensions of 9409T FDD

7.5.1 Drive Orientation

The 9409T can be mounted in any of the following loading positions:

- horizontal with the access door opening upward and PCB facing upward.
- vertical with the access door opening to the left or right.
- upright with the front panel at the top.

The drive should not be mounted with the PCB facing downward.

8.0 RECORDING CHARACTERISTICS/FORMAT

Capacity is determined by customer-selected data format and coding techniques.

8.1 ENCODING METHODS

Data can be recorded in either FM or MFM encoding. The format of the data recorded is a function of the host system.

8.1.1 Single-Density Recording

Double-frequency modulation (FM) recording is recommended for use in the single-density mode. FM recording is self-clocking and provides synchronization for data separation utilizing simple one-shot techniques. However, use of a phase-lock oscillator (PLO)* instead of a simple one-shot system will increase operating margins and result in greater data reliability with more tolerance for media imperfections.

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* PLO and Write Precompensation Application Note is available on request.

8.1.2 Double-Density Recording

Modified frequency modulation (MFM) recording doubles the data storage capacity. Since the MFM coding technique is not self-clocking, it is necessary to use a PLO to generate a synchronized clock from the data stream. If both single- and double-density system are being used, the same PLO serves both applications. Improved window margins will result if precompensation is used during writing in order to limit the effective peak shift in the read-back signal.

8.1.2.1 Write Precompensation

Write precompensation is required to decrease the effect of bit shift on the reduced bit cell and recovery window timing of MFM data. The window is defined as being the total time allowed for the bit to appear and be recognized. The data recovery window of MFM is two microseconds as opposed to the FM window of four microseconds. The amount of recommended write precompensation for maximum window margin is 250 nanoseconds, early or late, in relation to nominal. Refer to Figure 5.

Write precompensation should be applied to tracks, 43 through 79, on both sides of the diskette. Switching in write precompensation by the controller is required.

Write precompensation is applied to data patterns that will result in a large amount of bit shift. The controller precompensation circuit looks at three bits on each side of a reference bit and determines whether or not to shift.

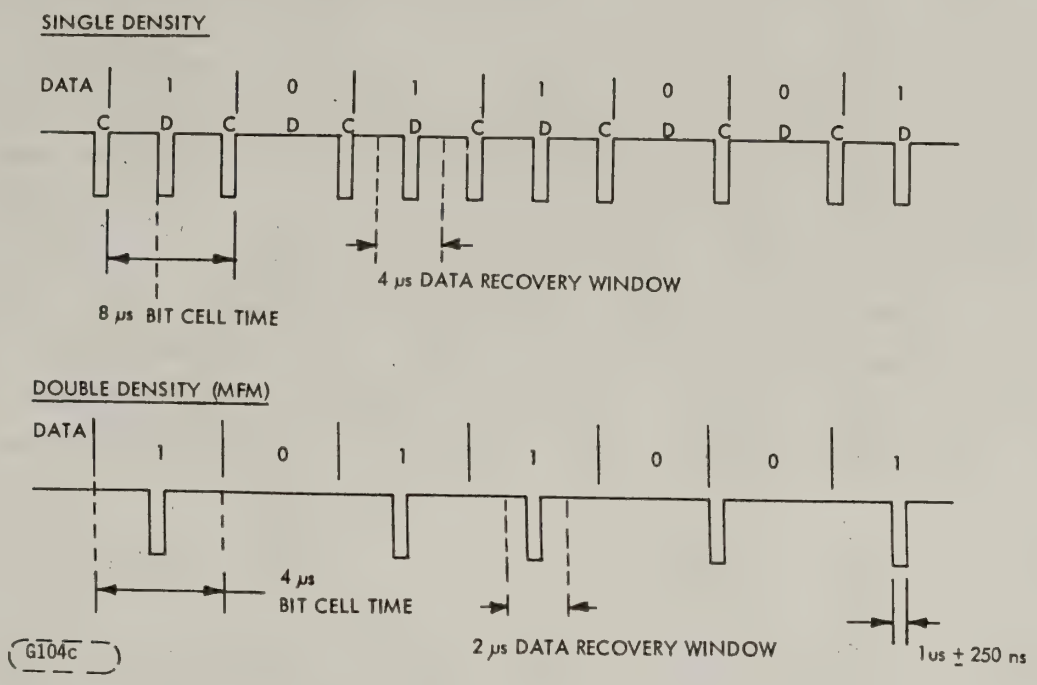


Figure 5. Nominal Data Timing

The following MFM patterns are compensated (bit-shifted) in the direction of the arrow.

LATE	EARLY
X 0 1 1	X 1 1 0
1 0 0 0	0 0 0 1

X = Don't Care

The following is an explanation of the MFM write precompensation algorithm.

When a data pattern of 011 is written on the disk, the first 1 is shifted toward the 0 (data bit cell with or without flux transition). Write precompensation shifts this 1 in the opposite direction the amount of the expected shift. In the case

of the 1000 pattern, the second 0 (clock bit) shifts toward the first 0 (data bit cell with no flux transition) and this clock bit is compensated late towards the third 0 (clock bit). With pattern 110, the second 1 shifts toward the 0 (bit cell with no transition) so this 1 data bit is compensated early towards the first 1 data bit. In the last pattern, 0001, the third 0 (clock bit) is shifted towards the 1 (data bit) due to the nominal 6 microseconds between these two bits. Thus, the third 0 (clock bit) is compensated early towards the second 0 to counteract shifting towards the 1.

8.2 FORMAT CONSIDERATIONS

Design of the 9409T allows for data recording using either hard or soft sector formats. The following operational tolerances should be considered when selecting a particular format for the system. For additional information, consult the Application Note, 5.25-Inch FDD Format Considerations and Controller Compatibilities, 75897469.

8.2.1 Index Tolerance

8.2.1.1 Post-Index (Gap No. 1)

Before initial recording of data upon a selected track, a minimum gap time of 1 millisecond is required to allow for drive-to-drive and adjustment tolerances. This is the gap (Gap 1) from the edge of the index pulse to the beginning sync field for the ID field address mark. This gap allows for variations in Index pulse width, speed variations, and interchange tolerances between drives.

8.2.1.2 Pre-Index (Gap No. 4)

The Pre-Index Gap No. 4 is required to compensate for maximum speed variations between drives. Physically, the gap is the space between the last sector and beginning of the index pulse. Its minimum length is 7.2 milliseconds in the recommended formats.

8.2.2 Inter-Record Tolerance

8.2.2.1 Pre-Address (Gap No. 3)

The Pre-address length is a minimum of 1.64 milliseconds, but varies with sector size for 128-byte sector lengths. The pre-address gap timing is Gap No. 3 and is based on the tunnel-erase structure of the read/write head and maximum erase-circuit turn-off delay.

8.2.2.2 Pre-Data (Gap No. 2)

Pre-data gap is Gap No. 2 and has a minimum timing requirement of 489 microseconds. Gap timing is determined by the erase turn-on circuit tolerance and the tunnel-erase structure of the read/write head.

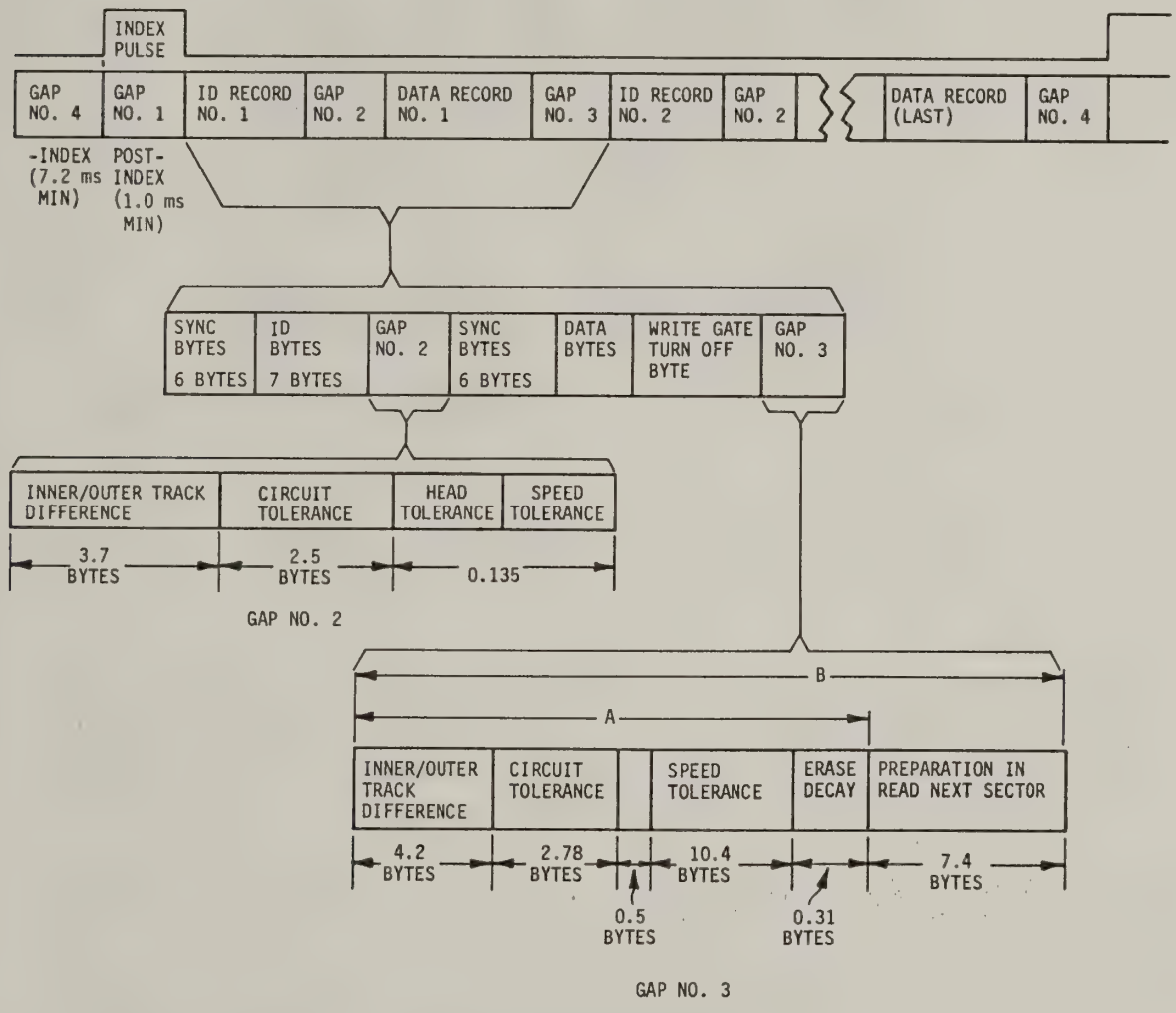
8.2.3 Soft-Sector Formatting

For system use of soft-sector formatting, Figure 6 provides several recommended timing tolerances for individual gaps positioned within the format. For sector formats utilizing MFM recording, Figure 7 presents the minimum gap for timing tolerances required for this recording scheme.

8.2.4 Hard-Sector Formatting

Hard-sector formats use sector holes in the diskette to separate the track into sectors. The mechanical and electrical parameters of flexible disk drives and media require the format to consist of three parts: Preamble, User Data, and Postamble.

The Preamble consists of a defined number of gap bytes that are written starting at the beginning of the sector pulse. The Preamble length is defined so that under worst-case conditions User Data will not be lost due to sector pulse jitter or erase delays.



A - 18.2 BYTES - TO PREVENT DATA LOSS UNDER WORST-CASE CONDITIONS.

B - 25.6 BYTES - GUARANTEES CONSECUTIVE SECTOR OPERATION UNDER WORST CASE CONDITIONS.

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Figure 6. Minimum Requirements for Single-Density Soft-Sector Format (Part 1)

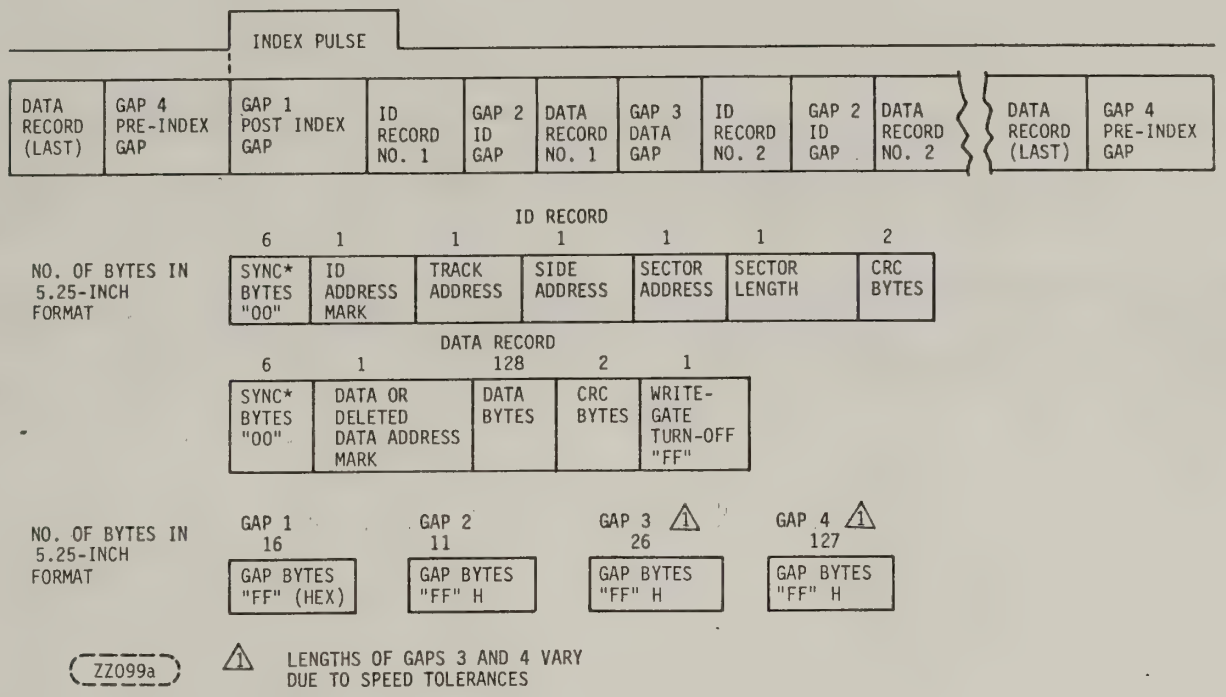
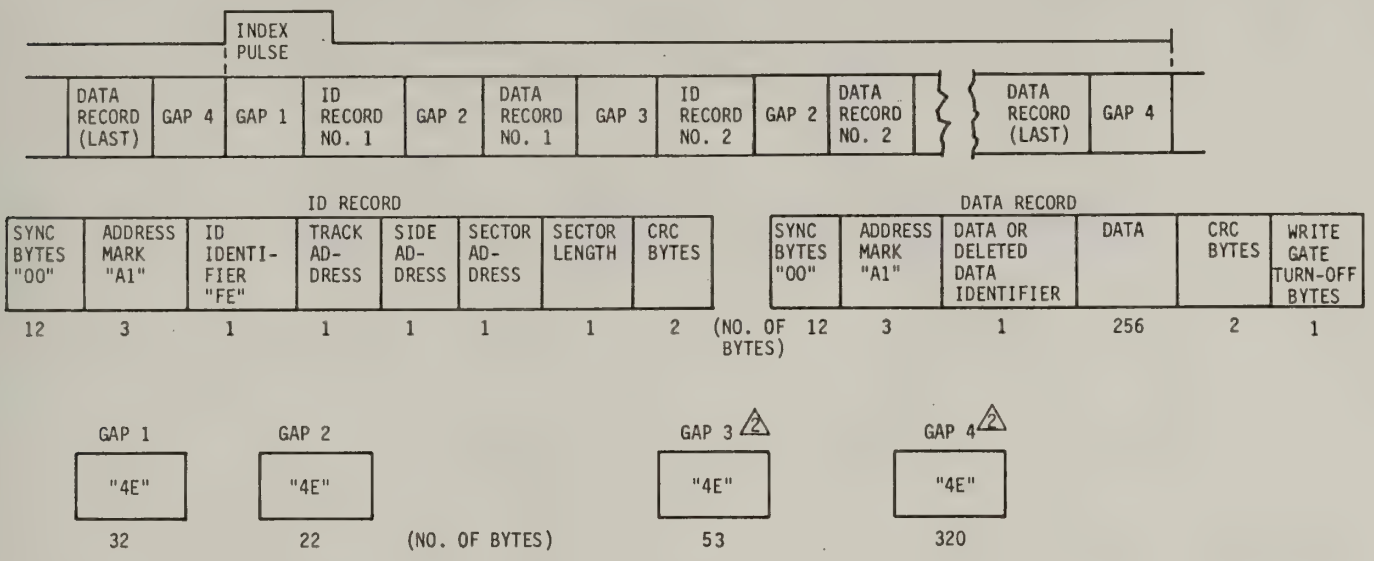

INDEX PULSE
DATA RECORD (LAST)
GAP 4 PRE-INDEX GAP
GAP 1 POST INDEX GAP
ID RECORD NO. 1
GAP 2 ID GAP
DATA RECORD NO. 1
GAP 3 DATA GAP
ID RECORD NO. 2
GAP 2 ID GAP
DATA RECORD NO. 2
DATA RECORD (LAST)
GAP 4 PRE-INDEX GAP
ID RECORD
NO. OF BYTES IN 5.25-INCH FORMAT
6 SYNC* BYTES "00"
1 ID ADDRESS MARK
1 TRACK ADDRESS
1 SIDE ADDRESS
1 SECTOR ADDRESS
1 SECTOR LENGTH
2 CRC BYTES
DATA RECORD
6 SYNC* BYTES "00"
1 DATA OR DELETED DATA ADDRESS MARK
128 DATA BYTES
2 CRC BYTES
1 WRITE-GATE TURN-OFF "FF"
NO. OF BYTES IN 5.25-INCH FORMAT
GAP 1 16 GAP BYTES "FF" (HEX)
GAP 2 11 GAP BYTES "FF" H
GAP 3 ⚠1 26 GAP BYTES "FF" H
GAP 4 ⚠1 127 GAP BYTES "FF" H
ZZ099a
⚠1 LENGTHS OF GAPS 3 AND 4 VARY DUE TO SPEED TOLERANCES

Figure 6. Minimum Requirements for Single-Density Soft-Sector Format (Part 2)

User Data consists of data, sync bytes, ID bytes, and CRC bytes used by the particular format. User Data and the Preamble are both written each time a sector is updated.

A buffer zone, or Postamble, is required at the end of a sector between the User Data and the earliest sector pulse.

Recommended minimum Preamble and Postamble gaps are given in Table 2 and illustrated in Figure 8.



1 SHOWN FOR 16-256 BYTE SECTORS.

2 LENGTHS OF GAPS 3 AND 4 VARY DUE TO SPEED TOLERANCES.

ZZ099c

Figure 7. Recommended Double-Density Format

Table 2. Recommended Preamble/Postamble Gap

POSTAMBLE		BLANK (NO CHARACTER WRITTEN)	ZEROES (CHARACTER WRITTEN)
16 Sectors Per Track	Minimum Preamble	8 bytes	24 bytes
	Maximum User Data	156 bytes	148 bytes
	Minimum Postamble	22 bytes	15 bytes
10 Sectors Per Track	Minimum Preamble	8 bytes	23 bytes
	Maximum User Data	269 bytes	261 bytes
	Minimum Postamble	27 bytes	19 bytes

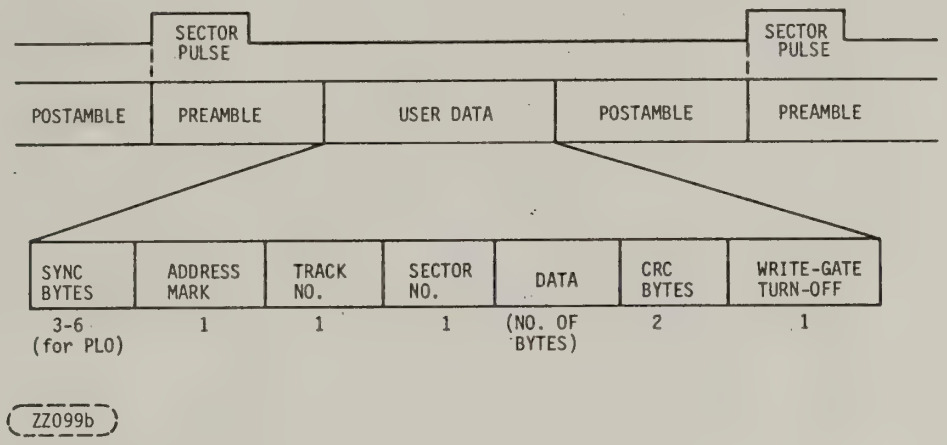


Figure 8. Recommended Hard Sector Format

As shown in Table 2, there are two ways to configure the Postamble Field: Blank and Zeroes.

1. Blank (No Character Written) - the controller can turn off Write Data at the end of the User Data field and leave the Postamble as an empty or blank field.

2. Zeroes (Character Written) - the Write Gate can turn off Write Data at the beginning of the next sector pulse. When doing this, the controller must write gap characters; that is, all zeroes in the Postamble field.

The Write Gate Turn-Off at the end of the User Data field is recommended because it allows the use of a larger User Data field. The values given for maximum User Data field guarantee maximum recovery for read-after-write operation under worst-case conditions.

9.0 INSTALLATION INFORMATION

9.1 ELECTRICAL INTERFACE

The electrical interface between the 9409T and host system consists of two primary connectors. The I/O signal connector J1 contains all interface signals transmitted to and from the drive. Connector J2 supplies DC power to the 9409T. AC power is not applicable to this device. A separate frame ground connection is available at the rear of the unit.

See Figure 9 for interface connections and Figure 10 for connector locations.

9.2 POWER CONNECTOR

DC power is provided to the 9409T by the host system through connector J2, which is mounted on the non-component side of the printed circuit board near the spindle drive motor. Refer to Figure 10 for connector location and Table 3 for pin assignments. Table 4 lists the recommended mating connector for J2.

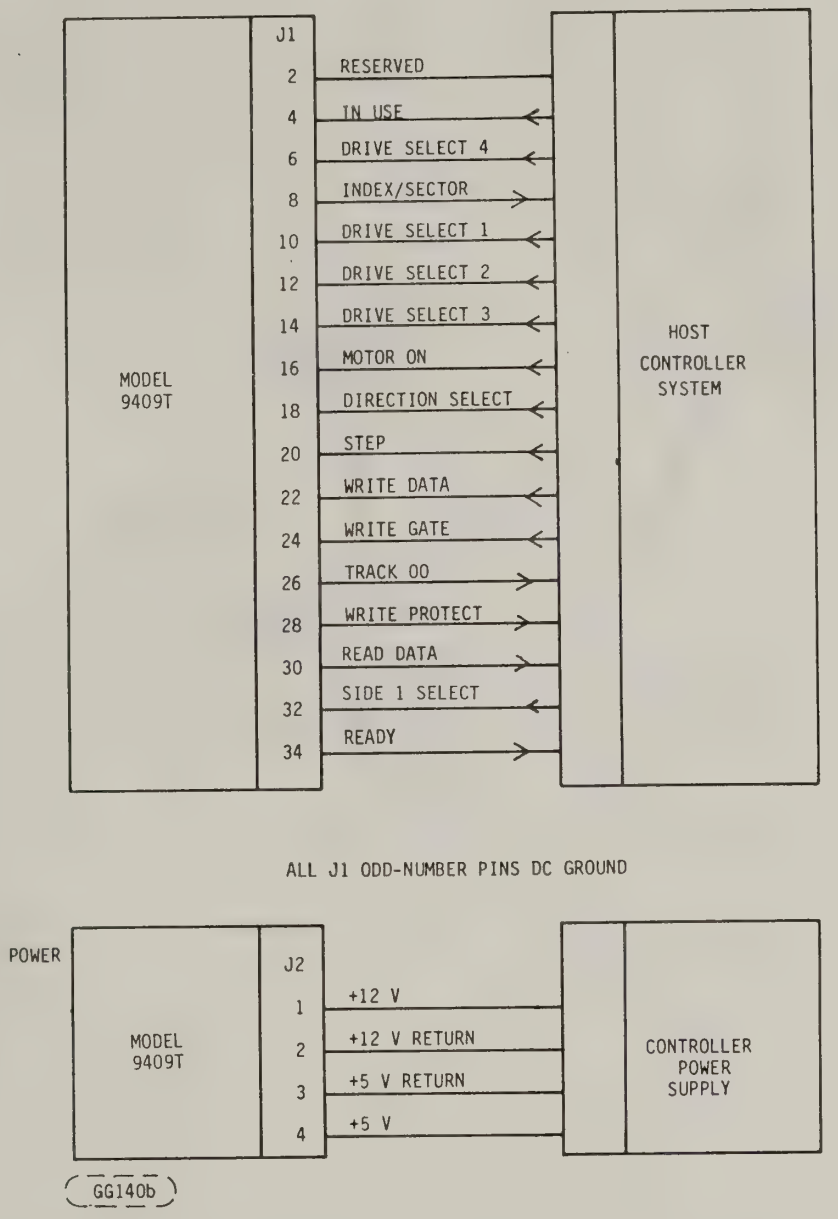


Figure 9. Interface Connections

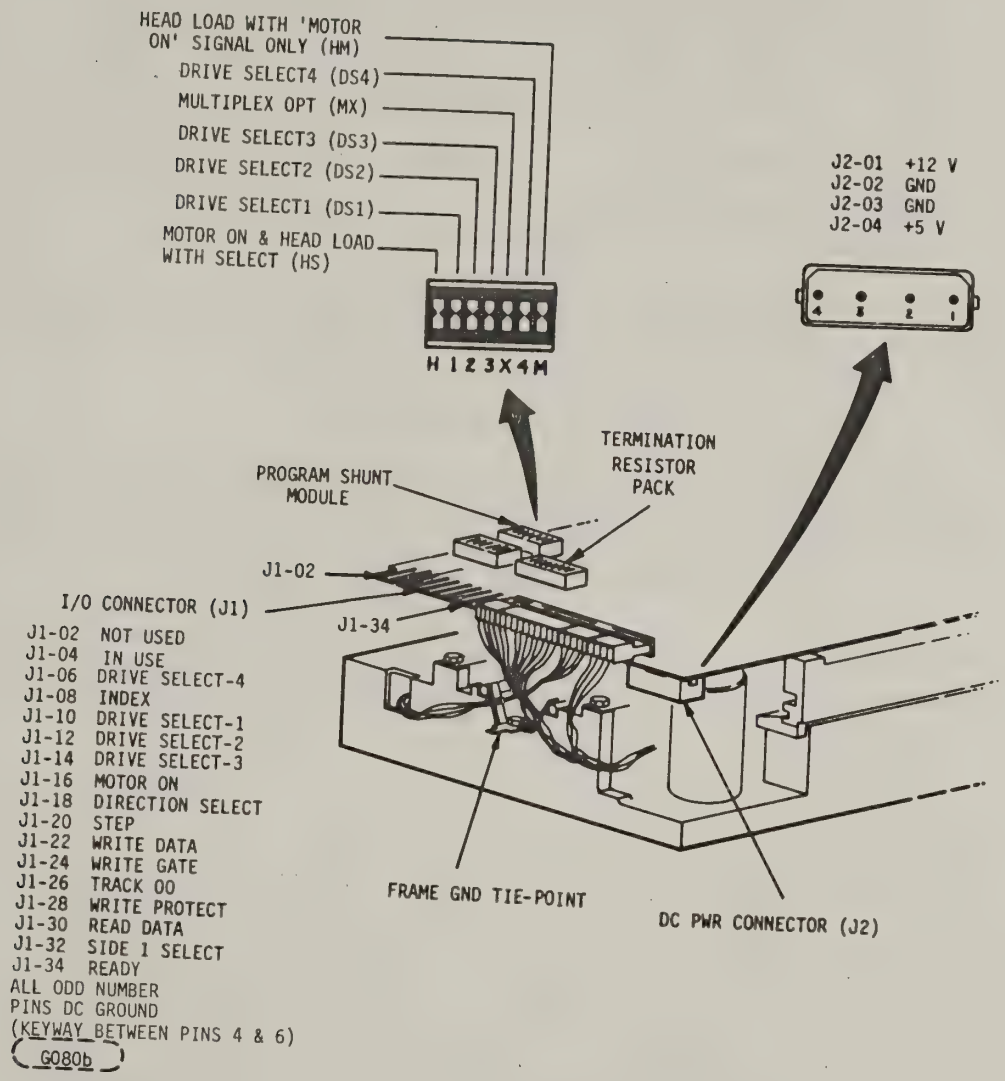


Figure 10. Input/Output (J1), DC Power (J2), Terminator, and Programmable Shunt Module Location/Description

Table 3. DC Interface

POWER LINE DESIGNATION	PIN NUMBER
+12 Volts	J2-01
+12 Volts Return	J2-02
+5 Volts Return	J2-03
+5 Volts	J2-04

Listed in Table 4 is connector information for J2/P2.

Table 4. J2/P2

TYPE OF CABLE	CONNECTOR	CONTACTS
18 AWG	J2, 4-Pin AMP Mate-N-Lok 350211-1 P2, AMP 1-480424-0	AMP 61473-1

9.3 I/O CONNECTOR

The I/O connector J1 is a 34-pin PCB edge connector. Its location is shown in Figure 10. The dimensions for J1 are shown in Figure 11. The pins are numbered 1 through 34, with the even-numbered pins appearing on the component side of the PCB and odd-numbered pins on the non-component side. A key slot is provided between pins 4 and 6 for optional connector keying.

The maximum I/O cable length between the host controller and the 9409T (or last FDD in a daisy chain configuration) should be no greater than 10 feet (3.048 meters). Refer to Section 9.5 for more detailed information.

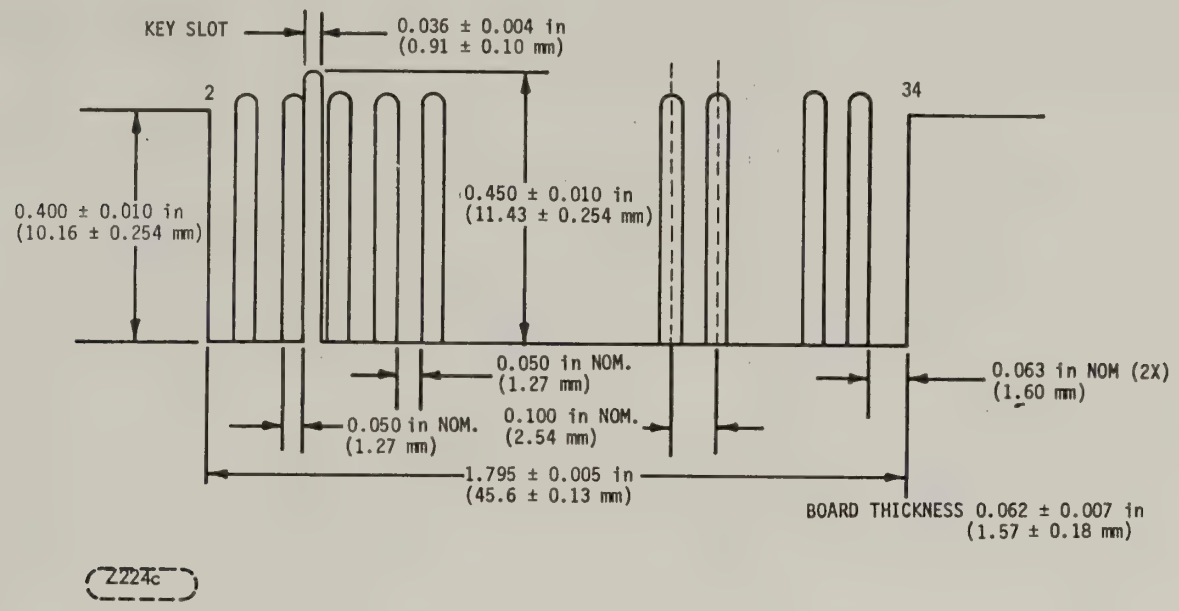


Figure 11. I/O Connector (J1) Dimensions

The recommended mating connector for J1 and type of cable are shown in Table 5.

Table 5. J1/P1

TYPE OF CABLE	CONNECTOR	CONTACTS
Twisted Pair, 26 AWG	AMP 583717-5	AMP 1-583616-4
Flat Cable	3M Scotchflex 3463-0001	---
---	AMP Keying Pin 583274-2	---

9.4 GROUNDING REQUIREMENTS

To ensure optimum performance and noise immunity, the 9409T must be frame grounded to the host equipment AC ground. A Faston tab has been provided on the rear of the casting where its mating Faston connector can be attached or soldered. The tab is AMP part number 61664-1 and its mating connector is AMP part number 60972-1. Figure 10 shows the ground point.

9.5 CONFIGURATIONS

9.5.1 Daisy-Chain Configuration

A daisy-chain configuration incorporates interfacing of the disk drives on a common I/O cable. Only the FDD which is selected by the host system has its control and data signals enabled through this common interface. The program shunt module shown in Figure 10 allows creation of each individual drive-selection address for each drive in the daisy-chain. Four drive selection addresses are made available by the program shunt module for interfacing up to four drives in a daisy chain configuration (shown in Figure 12).

Refer to section 12.0 for descriptions of drive selection and head load options.

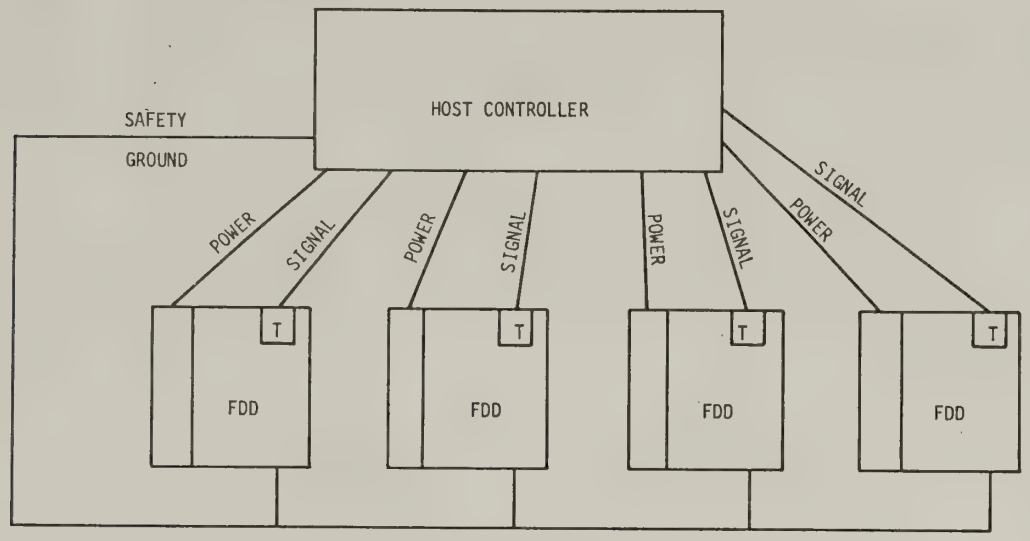
Termination in a daisy chain configuration is described in paragraph 9.6.3.

9.5.2 Radial Configuration

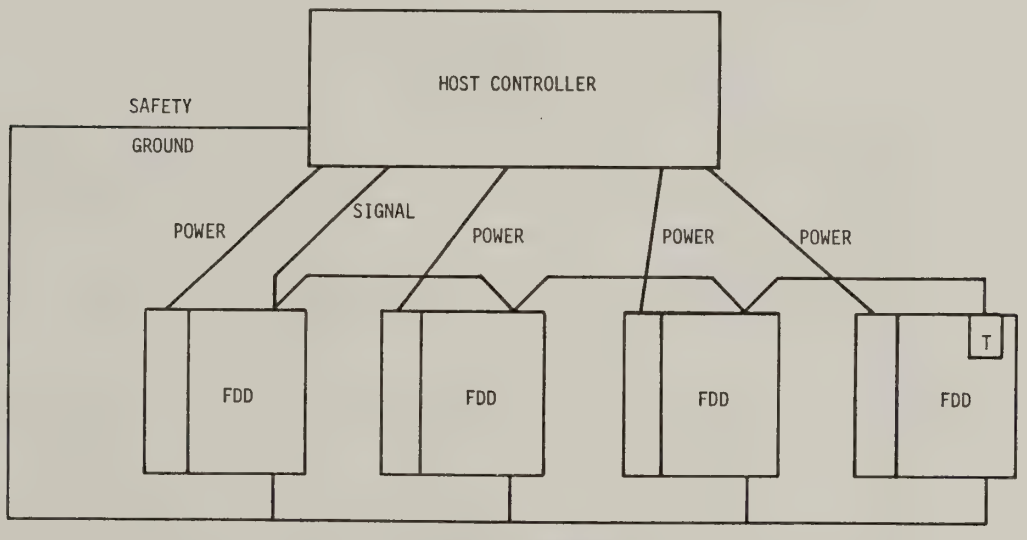
In a radial configuration the disk drives do not share the same I/O cable. Each drive is interfaced to its own I/O cable which, in turn, allows interfacing of more than four drives and a variety of system operational techniques. Drive-selection addressing must be accommodated at the program shunt module to allow activation of I/O signals.

Refer to section 12.0 for descriptions of drive select and head load options.

A radial configuration is shown in Figure 12 and termination is described in paragraph 9.6.2.



RADIAL CONFIGURATION



DAISY-CHAIN CONFIGURATION

P10122

T INDICATES PRESENCE OF RESISTOR TERMINATOR PACK.

Figure 12. FDD System Connection Configurations

9.6 INTERFACE TERMINATIONS

Figure 13 provides a logical representation of the interface line termination used for the 9409T.

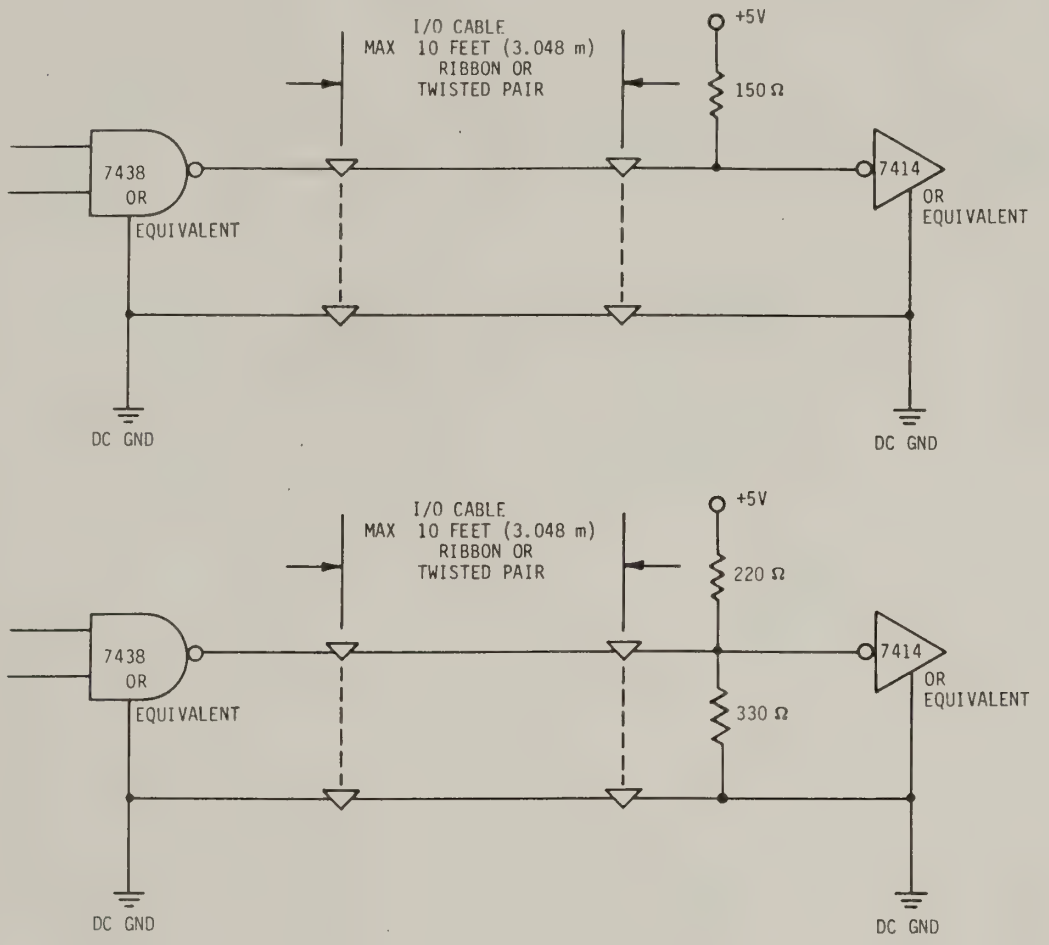


Figure 13. Interface Terminations

9.6.1 Areas of Termination

Termination for each input line is accommodated by a resistor pack installed in a DIP socket located on the PCB of the 9409T (Figure 10). The configuration and value of the termination resistors is determined by the PWA type, see Figure 13.

9.6.2 Termination in a Radial Configuration

In a single drive or radial configuration, the resistor pack must be kept in place on each PCB to provide the proper terminations.

9.6.3 Termination in a Daisy Chain Configuration

In a daisy chain configuration, only the last drive on the interface is to be terminated. All other drives on the interface must have the resistor pack removed.

9.6.4 External Terminations

For configurations requiring external termination, the user must terminate each input line to +5 V dc through a 150-ohm, 1/4-watt resistor.

10.0 ERROR RECOVERY

Seek errors will rarely occur unless the stepping rate is exceeded. In the event of a seek error, recalibration of track location can be achieved by repetitive step-out commands until a Track 00 signal is received.

To guard against degradation from imperfections in the media, no more than four attempts to write a record should be attempted when read-after-write errors are encountered. If a record cannot be successfully written within four attempts, it is recommended that the sector or track be labeled defective and an alternate sector or track assigned. If more than two defective tracks are encountered, it is recommended that the diskette be replaced.

In the event of a read error, up to 10 attempts should be made to recover with reread operations. If after 10 attempts the data has not been recovered, step the head several tracks away and then reposition to recover the data. Unloading the head when data transfers are not imminent will increase the data reliability and extend diskette life.

11.0 INTERFACE SIGNAL DESCRIPTION

11.1 ACTIVE/INACTIVE LOGIC SIGNALS

Signal State	Logic Level	Voltage
Inactive (False)	High	+2.5 V to +5.25 V
Active (True)	Low	0.0 V to +0.4 V

11.2 INPUT/OUTPUT SIGNALS

11.2.1 Drive Select

Drive Select (J1-6, -10, -12, -14) activates the internal circuitry of a selected drive. Activating this line to a logic low (active) level will condition the drive's input and output lines. All input and output lines are gated with Drive Select with the exception of Motor On (J1-16) and In Use (J1-4).

After the activation of the Drive Select line, a minimum time delay is required before the start of any write or read operation. (See Figures 15 and 22.) Table 6 includes these minimum time delays which are dependent on the drive shunt configuration.

Table 6. Minimum Time Delays

MODE OF OPERATION	TIME TO VALID READ DATA
Motor up to speed and head loaded (with or without head load option).	2 microseconds
Optional head load.	50 milliseconds
Motor on when drive selected.	150 milliseconds typical

The operation of the Drive Select lines and selection of a designated drive is controlled through the programmable shunt position DS1, DS2, DS3, and DS4. Refer to section 12.0 for further information.

11.2.2 Motor On

The Motor On circuit can be configured to operate in any of the three different ways described below.

1. If shunt HM is shorted and HS is open, the drive motor will turn on and the head will load when a logic low is applied to the Motor On line (J1-16). There is a 150-millisecond delay from active Motor On until there is valid read data.

   a. The advantage of this configuration is that after initial motor up-to-speed delay, the drive can be selected (Drive Select line active) and there is a maximum of 150 milliseconds (typical) before valid read data. (Motor must be turned on for this to be valid; with or without the head load option.)

   b. The disadvantage of this configuration is that with the motor turned on and the head loaded at all times, there is increased wear to the drive motor, media, and heads.

2. If shunt HS is shorted and HM is open, the drive motor will turn on when a logic low is applied to any of the Drive Select lines (J1-6, -10, -12, or -14). This configuration uses the Drive Select line to start the motor and load the heads. The minimum delay from drive selection to valid read data is now 150 milliseconds (typical) due to the delay for motor start time.

   a. The advantage of this configuration is reduced motor, media, and head wear because motor, media, and heads are only used when needed (selected).

b. The disadvantage of this configuration is that the maximum time from drive selection to valid read data is 150 milliseconds.

3. Same shunt configuration as case 2; that is, HS shorted and HM open. However, the Motor On line, rather than the Drive Select line, is used to start the motor. In this case, if the head load option is used, the head is loaded when the drive is selected and a 50-millisecond delay is required before there is valid read data. If the head load option is not used, there is valid read data 2 microseconds after drive selection. (The above two timing intervals assume that motor-up-to-speed delay has been met.)

   a. The advantage of this configuration is that it can be used to obtain the maximum drive-to-drive access time in a daisy chain (assuming that the head load option is not used).

   b. The disadvantage of using the Motor On line to turn on the drive motor is that all drives in a daisy chain configuration turn on the motor when a low level is applied to Motor On.

11.2.3 Direction Select

Direction Select (J1-18) transfers a control signal to determine the direction the read/write head will move when the Step line is pulsed.

A logic high defines the direction as "out," and if a pulse is applied to the Step line, the read/write head will move away from the center of the diskette. Conversely, if this input is a logic low level, the direction of motion is defined as "in," and if a pulse is applied to the Step line, the read/write head will move toward the center of the diskette. Refer to Figure 14 for timing details.

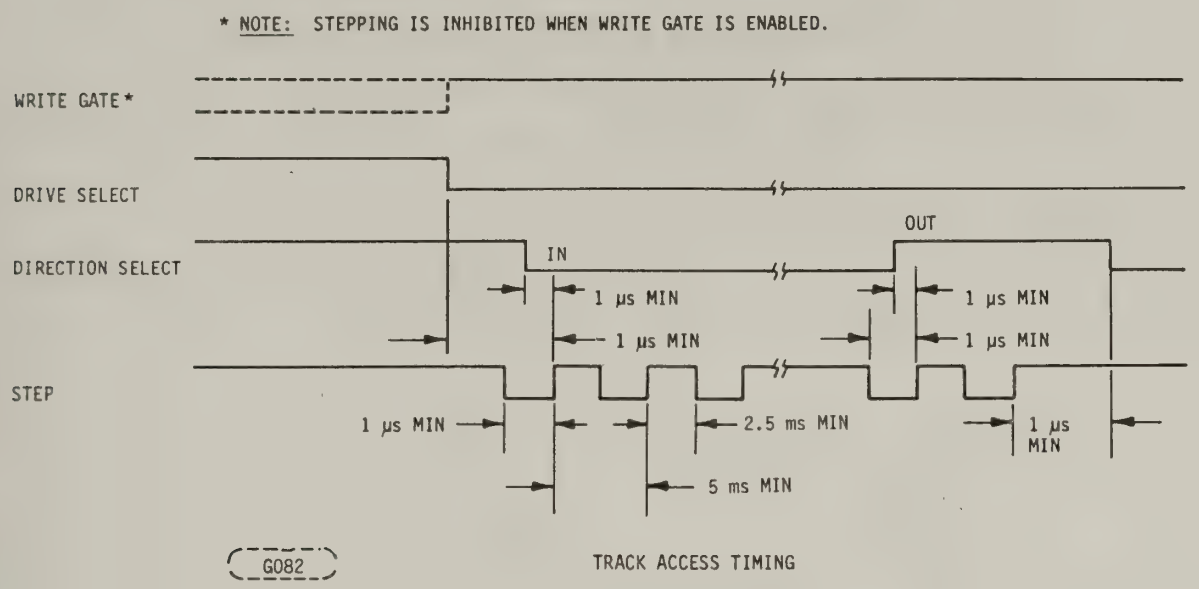


Figure 14. Track Access Timing

11.2.4 Step

Step (J1-20) pulses are control signals which cause the read/write head to move in a direction determined by the condition of the Direction Select line.

Access motion is initiated on each logic low-to-high transition, or on the trailing edge of each signal pulse. Any change in the Direction Select line must be made at least 1 microsecond before the trailing edge of the Step pulse. A requirement exists for the Direction Select logic level to be maintained 1 microsecond after the trailing edge of the Step pulse.

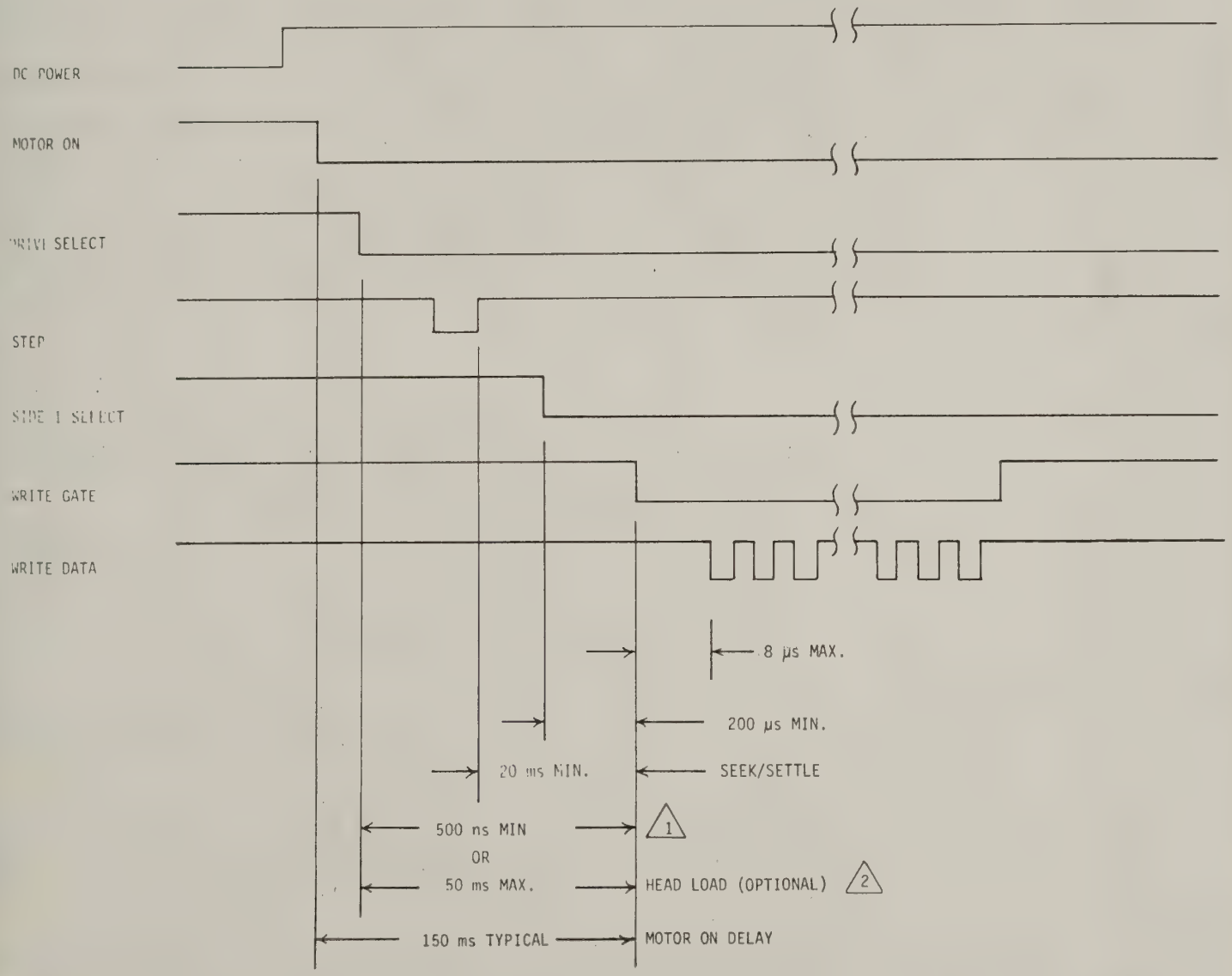
Activation of the Write Gate line while using a write-protected diskette will not inhibit movement of the read/write head during transmission of Step pulses.

Refer to Figure 14 for timing details.

11.2.5 Write Gate

The active state of Write Gate (J1-24), or logic low, enables Write Data to be written on the diskette. The inactive state, or logic high, enables the Read Data logic and Step logic.

A maximum delay time of 8 microseconds is allowed between the switching sequence of the Write Gate line and the leading edge of the first data pulse to be recorded. Figure 15 illustrates this sequence of events.



1 ASSUMES HEAD IS LOADED AND MOTOR IS UP TO SPEED WHEN DRIVE IS SELECTED.

GG142a 2 IF HEAD LOAD SOLENOID IS NOT USED, 500 ns MINIMUM.

Figure 15. Write Initiate Timing

11.2.6 Write Data

Write Data (J1-22) provides data to be written on the diskette. Each pulse transition from a logic high to a logic low level, as clocked through a D flip-flop within the logic circuitry, will cause current through the read/write head to reverse, creating a data bit.

Signals transmitted on the Write Data line are transmitted in the form of clock/data composite pulses. The recommended pulse width for both data bit and clock pulse is 200 nanoseconds (minimum) and 2.1 microseconds (maximum). Generation of data on the media is possible only during activation of the Write Gate to a logic low level. Figure 16 illustrates these timing sequences. Refer to paragraph 8.1.2.1 for recommended write precompensation.

11.2.8

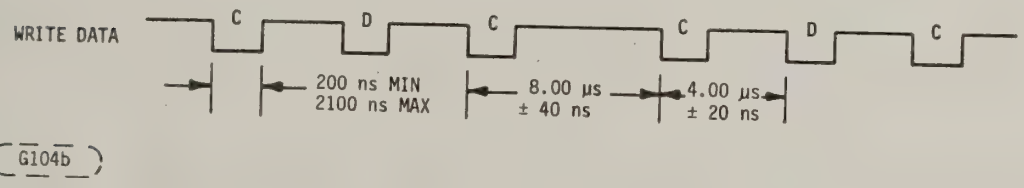


Figure 16. Write Data Timing (FM)

1.2.7 Read/Write Operations

At the conclusion of a write or read operation, there are a number of timing considerations which must be observed.

1. After any write operation, there is a 1-millisecond minimum time delay to allow for the erase turn-off delay required with the tunnel erase head. Interface signals which must

remain in a stable state during this delay are: a) Drive Select, b) Head Load, c) Motor On, d) Side 1 Select, and e) Step. This can be considered as write operation-to-read operation time.

2. If a side change occurs at the termination of a write operation, the side change delay of 200 microseconds plus the 1-millisecond erase turn-off delay is required; that is, a total of 1200 microseconds. This is write-to-read time including a side change.

3. In going from a read operation to a read operation including a side change, only the side change delay of 200 microseconds must be observed.

Refer to Figure 17 for detailed timing.

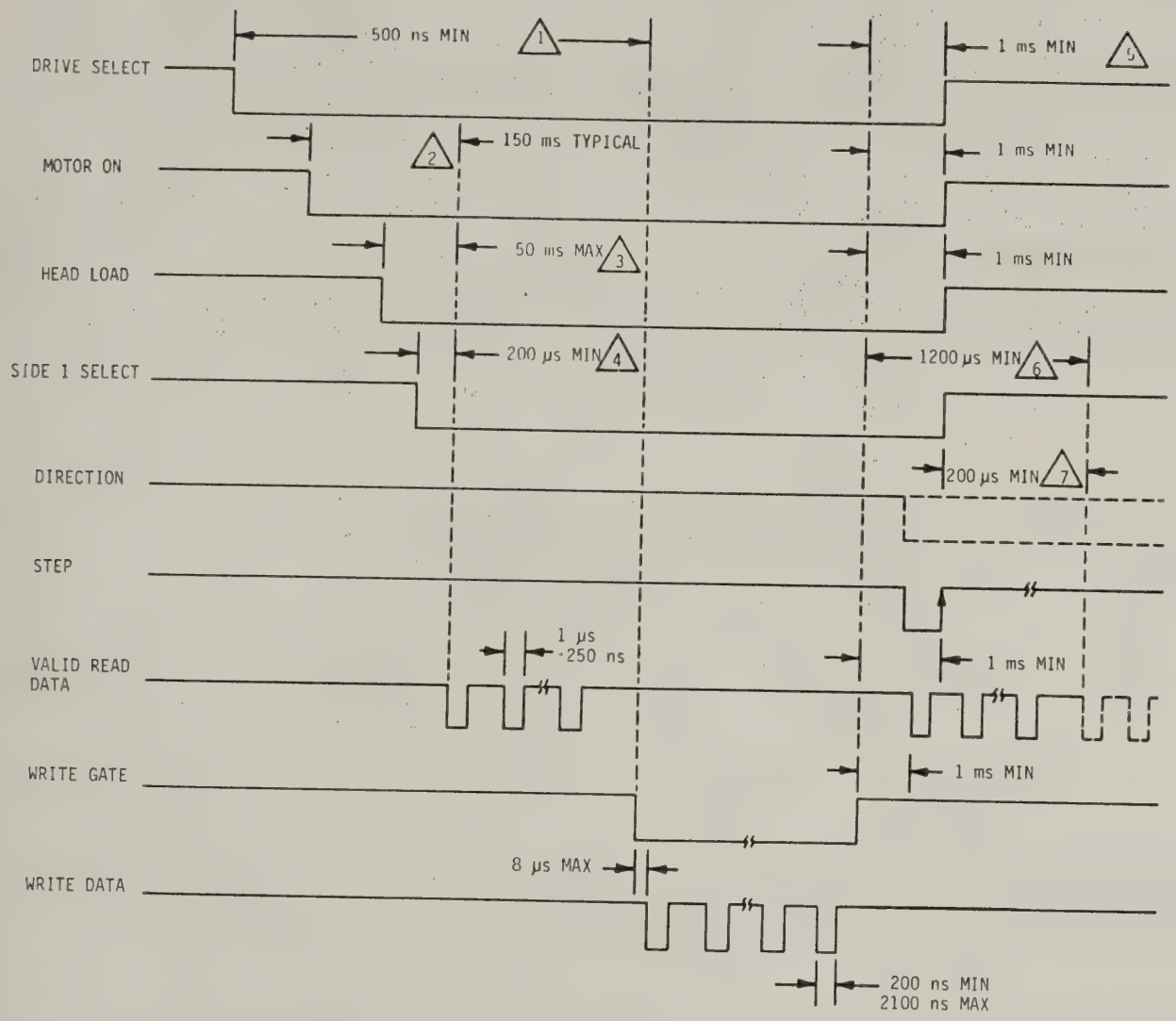
11.2.8 Track 00

The active or logic low state of the Track 00 signal (J1-26) indicates the read/write head is positioned at track 00.

This signal is at a logic high level (inactive state) when the read/write head is not at track 00.

When the read/write head is at track 00, and an additional step-out pulse is issued to the drive, motion is inhibited and the Track 00 signal will remain active (logic low).

A step-out sequence is recommended on a power-up sequence or a restore function to recalibrate for track 00 position.



1. ASSUMES MOTOR ON AND HEAD LOADED.
2. ASSUMES NO HEAD LOAD SOLENOID.
3. ASSUMFS MOTOR UP TO SPEED. (50 ms IF HEAD LOAD OPTION USED.)
4. ASSUMES MOTOR UP TO SPEED AND HEAD LOADED.
5. THE 1 ms IS THE ERASE TURN-OFF DELAY REQUIRED FOR TUNNEL ERASE HEADS.
6. THE 1200 µs IS THE ERASE TURN-OFF DELAY PLUS SIDE CHANGE DELAY.
7. THE 200 µs IS REQUIRED FOR A CHANGE IN SIDE CHANGE.

GG143a

Figure 17. Read/Write Operations

11.2.9 Index/Sector

The Index/Sector signal (J1-8) is detected and transmitted to the controller each time an index or sector hole is sensed by the index/sector photocell detector.

The signal generated is a 0.5 millisecond (minimum) pulse which indicates the presence of an Index or Sector hole during its transition from a logical one to a logical zero level as shown in Figure 18.

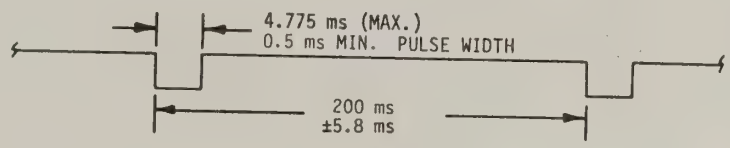


Figure 18. Index Timing (Soft-Sector Media)

Using soft-sectored media, a single pulse will be generated per revolution of the diskette, every 200 ±5.8 milliseconds, indicating the physical beginning of a track.

Using hard-sectored media (16 or 10 sectors), 17 or 11 pulses, respectively, will be generated per revolution. Figures 19 and 20 provide an illustration of index/sector timings for 16 and 10 sector applications.

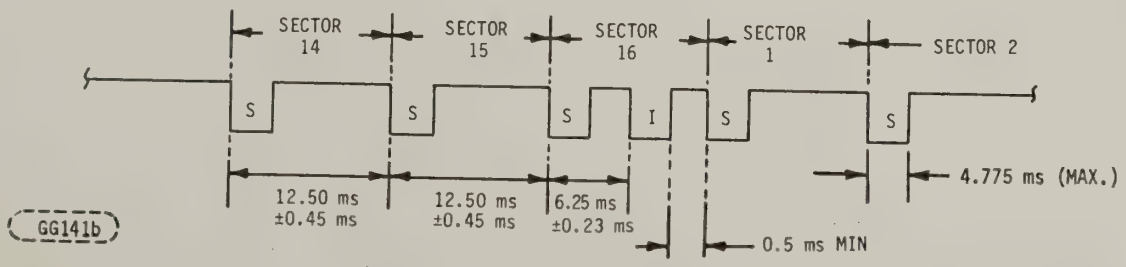


Figure 19. Index/Sector Timing (16 Hard-Sector Media)

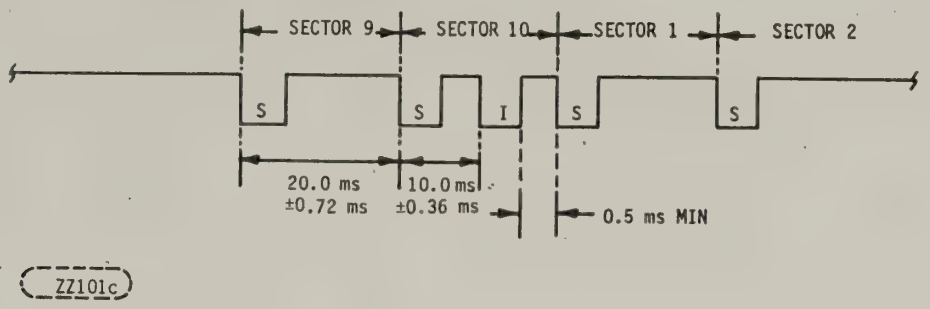


Figure 20. Index/Sector Timing (10 Hard-Sector Media)

11.2.10 Read Data

Read Data (J1-30) provides a transmission of composite clock and data pulses of 1 microsecond, ±250 nanoseconds, to indicate the presence of either a clock or data pulse by means of a logic high-to-low transition. Figures 21 and 22 provide references for timing and bit shift tolerance within normal media variations.

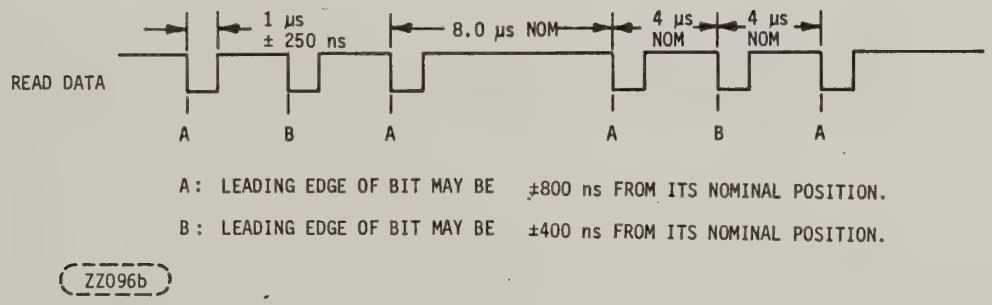


Figure 21. Read Signal Timing

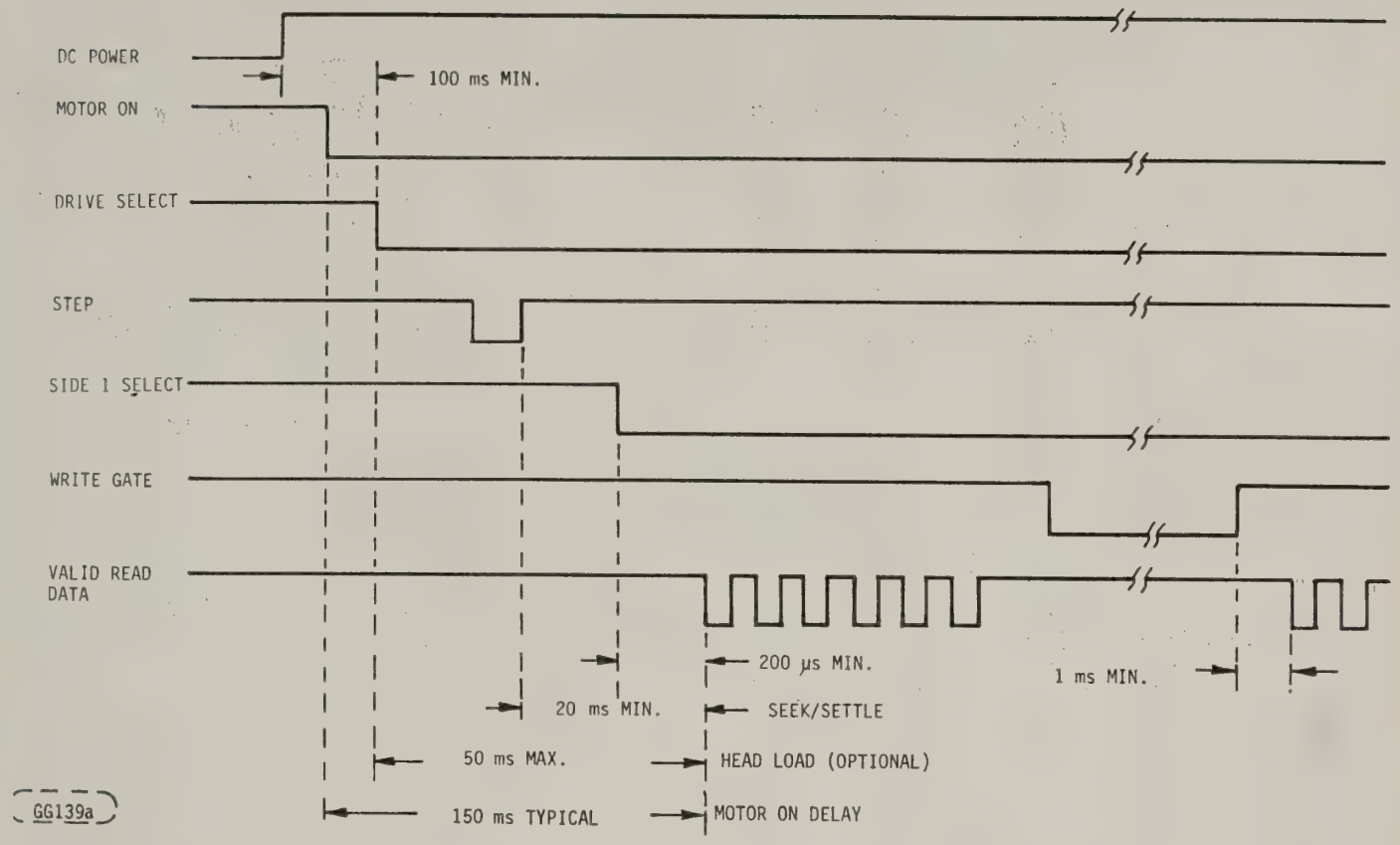


Figure 22. Read Initiate Timing

11.2.11 Write Protect

Write Protect (J1-28) notifies the user that a write protected diskette (i.e., when the write protect slot on the diskette is masked) is installed in the drive. The normal configuration is that a logic low level will appear on the interface line J1-28 indicating that the diskette is write protected and writing will be inhibited.

If it is necessary to invert this output signal so that an unmasked slot gives a write protect indication and inhibits writing, the user must move the black wire on the write protect

switch to the unused switch pin (the one closest to the PWA). This gives write protect indication to the I/O and inhibits writing on a diskette with an unmasked slot.

11.2.12 Side 1 Select

Side 1 Select (J1-32) defines which side of a two-sided diskette is used for reading and writing.

A logic high selects side 0, the lower surface; a logic low selects side 1, the upper surface. When the selected diskette side is changed, a delay of 200 microseconds is required before any read or write operation is initiated (assuming that drive is selected, motor is on, and head is loaded).

11.2.13 In Use

In Use (J1-4) allows for the activation of the activity LED independent of Drive Select. When a logic low is applied to In Use the activity LED is turned on whether or not the drive is selected. In daisy-chain operation, all drives would have the activity LED illuminated if In Use is active.

11.2.14 Ready Status/Door Closed Status Options

The significance of the signal generated by the device at the I/O connector J1-34 is determined by the configuration of the PWA (Printed Wire Assembly). In all configurations the signal at J1-34 is ACTIVE (Low) at the interface. The requirements of the controller to sense the FDD Door closed or that media is installed and spinning on a "Selected" device can be accommodated by present PWA configurations.

Example 1: HPC 77686000 (Figure A)

The signal "Door Closed" (J1-34) is a function of the FDD door being closed AND the device being "SELECTED". Note that "Door Closed" being TRUE indicates that the door is closed but does not indicate that media is in place.

Example 2: HPC 77711500/77711501/77711502 (Figure B)

The signal "Door Closed" (J1-34) is selected when the Zero-Ohm resistor is installed in position "W1". The same conditions apply as explained in Example 1.

The signal "Ready" (J1-34) is selected when the Zero-Ohm resistor is removed from "W1" and installed at "W3". This configuration can be used to insure that media is in place and spinning before the device is designated as "Ready".

Circuit function with Zero-Ohm resistor at "W3".

A. Control Signals:

1. Set inputs (S) to F/F-A and F/F-B pulled High via R10.
2. Data input (CD) to F/F-A pulled High via R10.
3. Data input (CD) to F/F-B a function of output (Q) of F/F-A.
4. Clock input (C) to F/F-A and F/F-B a function of INDEX/+L.

B. Operation:

1. Reset input (R) to F/F-A and F/F-B a function of DOOR CLOSED/+L Wire OR'ed with MOTOR ON. If the FDD door is opened or the motor is off F/F-A and F/F-B will be "Reset" and "Ready" will be FALSE (High). When the FDD door is closed and the motor is on the reset input (R) to F/F-A and F/F-B is High thereby allowing normal Flip/Flop action to occur.
2. The first "Index" pulse, after reset (R) is High, will set F/F-A.
3. The second "Index" pulse will set F/F-B.
4. The output (Q) from F/F-B is connected via "W3" to U5-4 where it is AND'ed with SELECT/+L. The output at U5-6 is True (Low) and appears as "Ready" at J1-34.

NOTE

The worst case condition would require a maximum of 550 milliseconds for the device to go "Ready" after the door is closed.

Example 3: HPC 77711503 (Figure C)

The signal "Ready" (J1-34) is selected when the Zero-Ohm resistors are installed at "W3" and "W5". This configuration can be used to insure that media is in place and spinning and a designated select sequence completed before the device will respond "Ready".

Circuit function with Zero-Ohm resistors at "W3" and "W5".

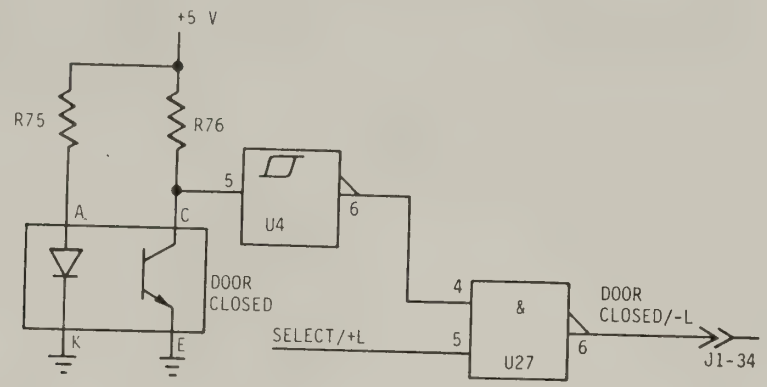
A. Control Signals:

1. Set inputs (S) to F/F-C and F/F-D pulled High via R10.
2. Data input (CD) to F/F-C pulled High via R10.
3. Clock input (C) to F/F-C a function of SELECT/-L.
4. Data input (CD) to F/F-D a function of set output (Q) from F/F-C via Zero-Ohm resistor at "W5".

5. Clock input (C) to F/F-D a function of INDEX/+L.
6. Reset inputs to F/F-C and F/F-D a function of DOOR CLOSED/+L and POR/-L.

B. Operations

1. Any time the FDD door is opened F/F-C and F/F-D will be Reset, causing the "Ready" term to be False.
   a) If the FDD is in a "Selected" state when the door is opened and then closed it will be necessary to "Deselect" then "Reselect" the device in order to set F/F-C. F/F-C being set is a requirement to set F/F-D.
   b) If the FDD is in a "Deselected" state when the door is opened and then closed it will be necessary to "Select", "Deselect", and "Select" the device in order to set F/F-C.
2. The set output (Q) of F/F-C is the data input (CD) to F/F-D. The first Index pulse after CD is High will set F/F-D.
3. The set output (Q) of F/F-D is connected via "W3" to U5-4 where it is AND'ed with SELECT/+L. The output at U5-6 is True (Low) and appears as "Ready" at J1-34

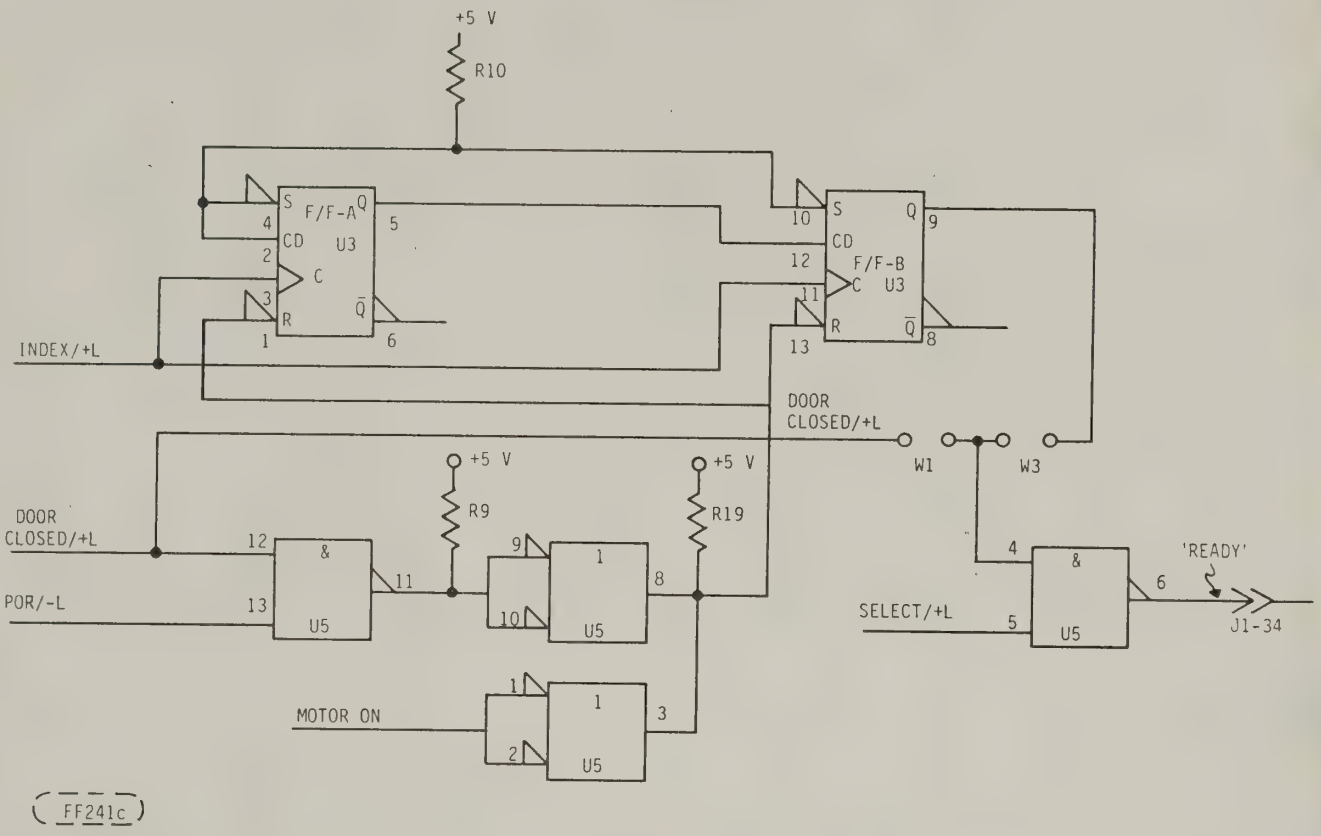


(FF241b)

HPC 77686000 (150 Ω Termination)

DOOR CLOSED (J1-34) provides an Active (Low) signal at the interface to indicate that the FDD Door is closed when the device is selected.

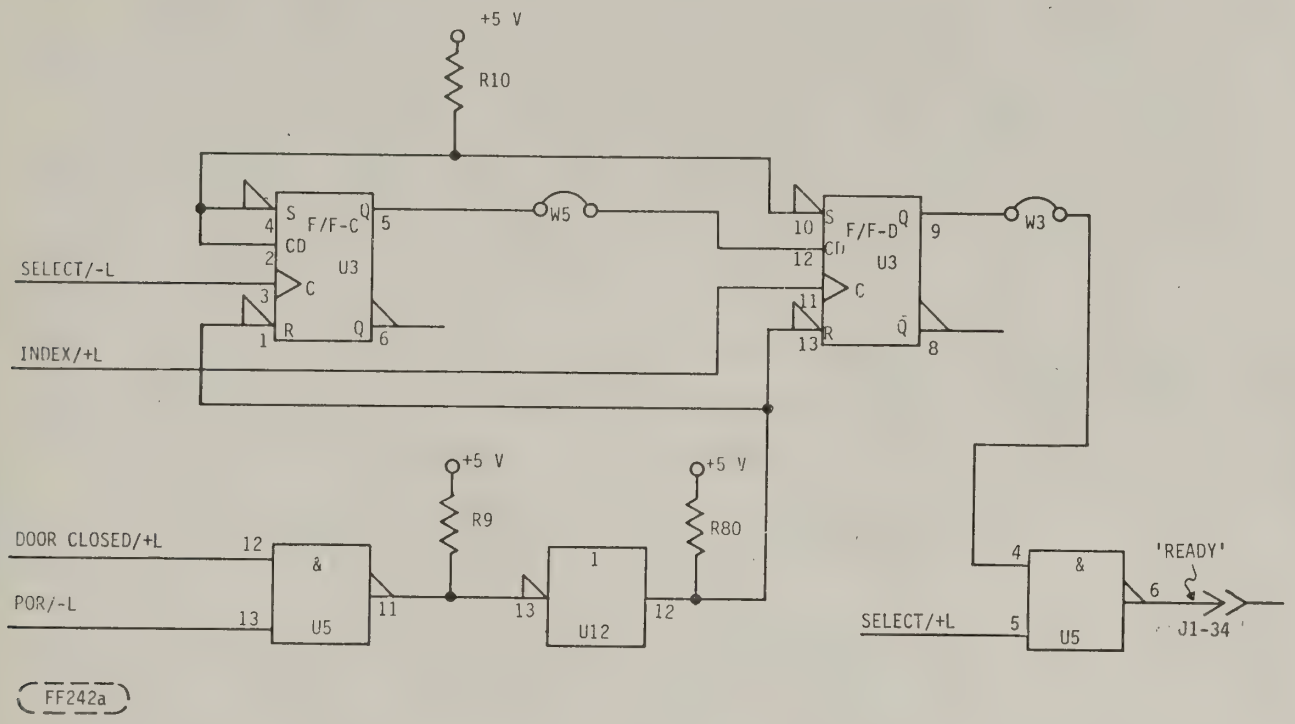
FIGURE A.



HPC 77711500 (220 Ω /330 Ω Termination)
HPC 77711502 (150 Ω Termination)
Zero-Ohm Resistor installed at "W1"
DOOR CLOSED (J1-34) provides an Active (Low) signal at the interface to indicate that the FDD Door is closed when the device is selected.

HPC 77711501 (220 Ω /330 Ω Termination)
Zero-Ohm Resistor installed at "W3".
READY (J1-34) provides an Active (Low) signal at the interface indicating that the FDD Door is closed, MOTOR ON is Active (Low), F/F-A and F/F-B are "Set" (result of 2 INDEX pulses) and the device is Selected.

FIGURE B.



HPC 77711503 (150Ω Termination)
Zero-Ohm Resistors installed at "W3" and "W5"
READY (J1-34) provides an Active (Low) signal at the interface indicating that the FDD Door is closed, F/F-D is set (result of 1 INDEX pulse) and the device is selected.

FIGURE C.

12.0 CUSTOMER SELECTABLE OPTIONS

The 9409T contains a 12-pin program shunt module mounted on the PWA (Figure 23) which allows the customer to configure the drive for single unit on multi-unit system operation. All of the shunts on the module are intact when shipped from the factory and it is necessary to program the module before the device is operated to avoid invalid configurations.

The program shunt module is AMP Part Number 435704-6. The shunt segments can be cut using an AMP cutting tool part number 1-435830-1. The program shunt module is installed in a DIP socket and, at the customer's option, can be replaced by a DIP switch part number AMP 435626-5.

The following paragraphs describe the various options (Table 7 provides a listing of those options) to assist the customer in selecting the features to be utilized.

12.1 MULTIPLEX OPTION

The 9409T is shipped from the factory configured to operate in a single drive system. To activate the multiplex option, cut MX (5-10) position of the programmable shunt. This will allow the multiplexing of I/O lines. For single drive applications, shorting MX will cause a constant enable on the I/O signal lines whether the drive is powered on.

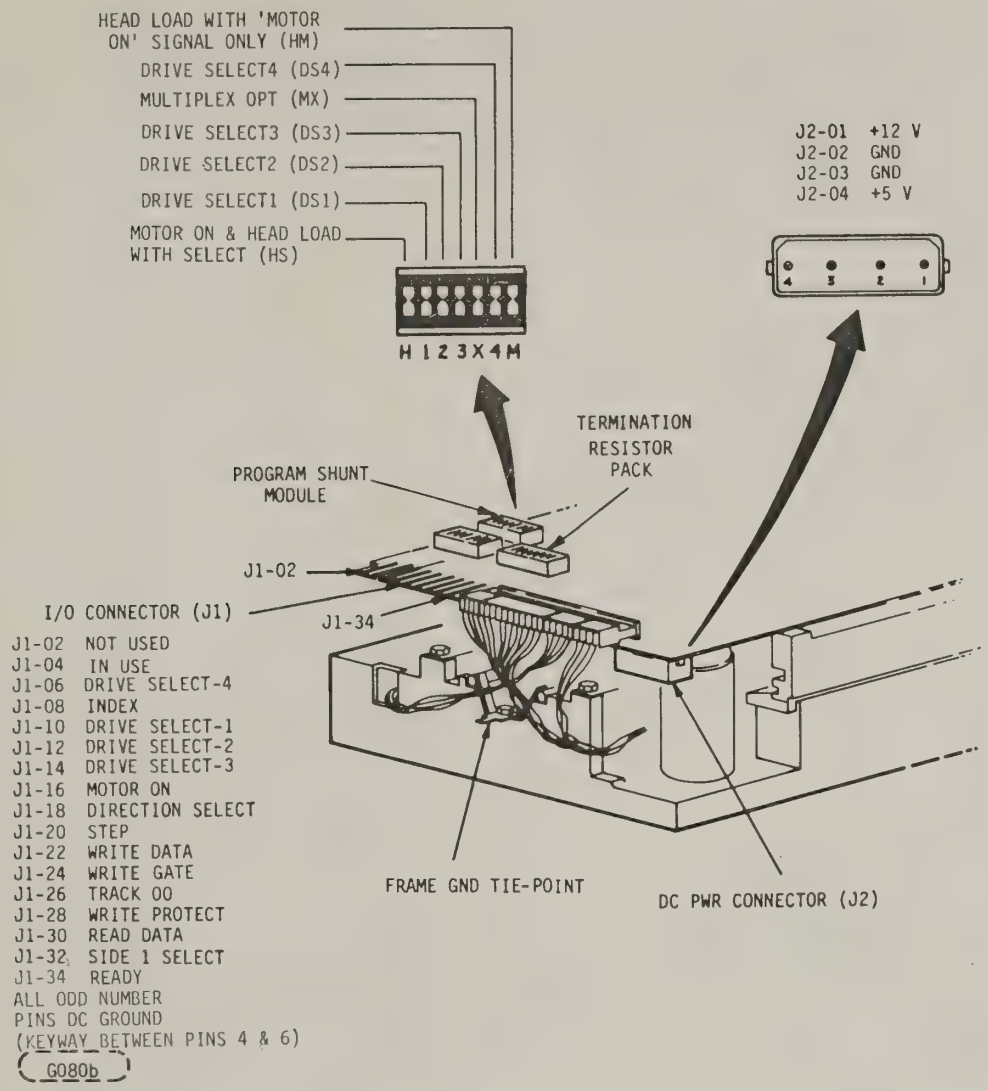


Figure 23. Program Shunt Module

12.2 DRIVE SELECT OPTIONS (1, 2, 3, 4)

The 9409T utilizes four input lines for designation of a particular drive. With MX (5-10) cut, positions DS1 through DS4 are used to select the Drive Select line which will activate the unique drive. Only the drive with its Drive Select line activated will respond to the input lines, gate the output lines, and turn on the indicator on the front panel. (Exception: the In Use line will turn on the indicator independent of all other lines.) For example, in designating a drive as Drive 1, the user must cut Drive Select shunts

DS2, DS3, DS4 (pins 3-12, 4-11, and 6-9, respectively) and leave DS1 (pins 2-13) shorted. Refer to Figure 24 for Drive Select shunt configurations.

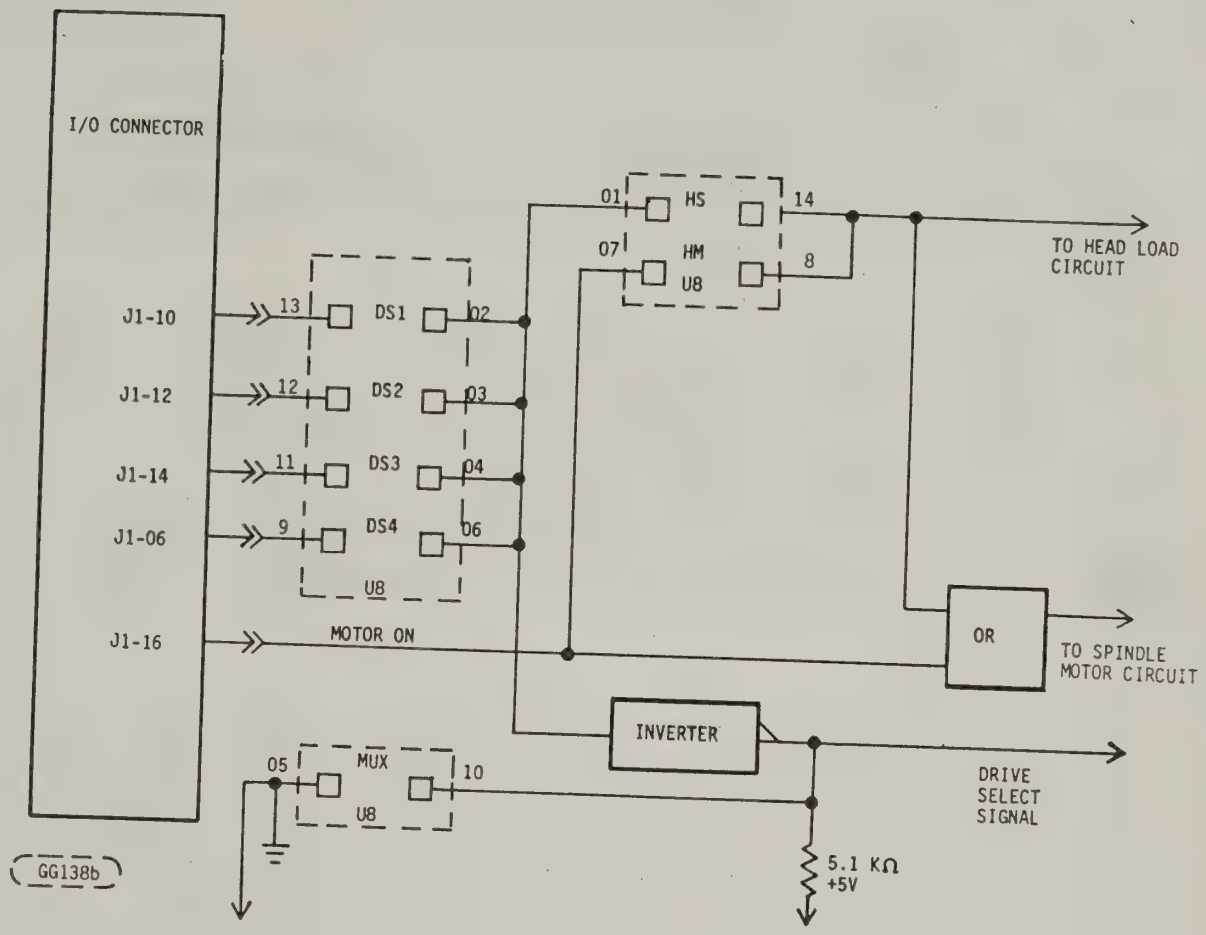


Figure 24. Drive Select Shunt Configuration

12.3 HEAD LOAD WITH MOTOR ON

With HM (7-8) shorted and HS (1-14) open*, the read/write head will load against the media when the Motor On line is activated to a logic low.

12.4 HEAD LOAD WITH DRIVE SELECT

With HS (1-14) shorted and HM (7-8) open*, the head load solenoid will energize with Drive Select activated and load the read/write head.

12.5 HEAD LOAD SOLENOID (Optional Feature)

In most applications, a head load/unload solenoid is not required. It is optional and can be supplied to customers on request. The head load solenoid option is recommended to extend media life and in all applications where it is impractical to turn the spindle motor off when the drive is not selected.

When this option is present (HS shorted, HM open), the solenoid may be activated and the heads loaded against the media when the drive is selected. With HM shorted and HS open, the solenoid will load when the Motor On line is activated to a logical 1 level. All read and write operations must be delayed for 50 milliseconds from the time of solenoid activation to permit the head to properly position itself against the media. This 50 milliseconds may be included in or added to motor start time.

*It is an invalid configuration to have both HS (1-14) and HM (7-8) shorted. In such a configuration, input current to Motor On and/or Drive Select may damage drivers on the host.

If the head-load solenoid is not used, the heads are loaded onto the media at all times. The drive spindle motor should be shut off when the file is not being accessed. This reduces media and drive motor wear.

Table 7. Customer Option Configurations

MX	HS	HM	DS1	DS2	DS3	DS4	NOTES
X	O	O	X	X	X	X	Invalid configuration. Head will not load.
O	O	S	S O O O	O S O O	O O S O	O O O S	• Read/write head is loaded and motor is turned on with a low level on Motor On. • Activity indicator activated (if In Use remains at a high level) and drive is selected by a low level on Drive Select.
O	S	O	S O O O	O S O O	O O S O	O O O S	• Read/write head is loaded, motor is turned on (if Motor On remains at a high level). • Activity indicator is activated (if In Use remains at a high level), and drive is selected by a low level on Drive Select.
S	O	S	S O O O	O S O O	O O S O	O O O S	• Drive is always selected. • Activity indicator is activated (if In Use remains at a high level) by a low level on Drive Select. • Heads load and motor is turned on with a low level on Motor On.
S	S	O	S O O O	O S O O	O O S O	O O O S	• Drive is always selected. • Read/write head is loaded, motor is turned on (if Motor On remains at a high level), and activity indicator is activated by a low level on Drive Select (if In Use line is held high).
X	S	S	X	X	X	X	Invalid configuration. Input current to Motor On and/or Drive Select may damage drivers on host.

S = SHORT O = OPEN X = DON'T CARE

If the head-load solenoid is not used, shunt positions HM and HS do not effect drive operation, ie., either may be used or both may be opened and there will be no performance change. In order to make the drive operational, only the desired drive select line need be shorted in the appropriate shunt position.